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The objective of this dissertation is to introduce low-cost processing methods for the fabrication of ZnO transparent thin-film transistors (TTFTs). A novel method for depositing ZnO body layers via spin-coating of a zinc nitrate-based spin solution is presented. The processing conditions of spin-coated ZnO are optimized to produce continuous and polycrystalline thin-films. Optimal spin-coated ZnO thin-films are obtained for a 32 nm thick film which is converted to ZnO at 600°C in air. Spin-coated ZnO TTFT mobilities are consistently in the range of 0.1 - 0.2 cm^2/Vs. Spin-coating deposition methods for HfO_2 are presented as a novel way to deposit low-cost gate insulators. Spin-coated HfO_2 dielectric has a breakdown field, dielectric constant, loss tangent, and leakage current at 1 MV/cm of $\sim$ 2.1 MV/cm, 12.1–13.5, 0.411%, and 17.37 nA/cm^2, respectively. Additionally, ZnO TTFTs constructed using spin-coated HfO_2 gate insulators possess electrical characteristics similar to those obtained with aluminum oxide and titanium oxide superlattice (ATO) gate dielectrics.

A second objective of this dissertation is to demonstrate a novel photolithography processing method for ZnO TTFTs with critical dimensions as small as 25 μm. Lithography patterning of ZnO TTFTs is introduced as a means of assessing the effects of shrinking device dimensions on electrical performance.

Low-Cost Deposition Methods for Transparent Thin-Film Transistors

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Benjamin J. Norris

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To my mother and father.

LOW-COST DEPOSITION METHODS FOR TRANSPARENT THIN-FILM TRANSISTORS

1. INTRODUCTION

The introduction of transparent thin-film transistors (TTFTs) by Hoffman *et al.* has generated a great deal of interest. [1, 2] TTFTs are of interest as a replacement to amorphous silicon thin-film transistors (TFTs) currently utilized in liquid-crystal displays (LCDs). Preliminary research indicates that ZnO TTFTs are well-suited and compatible with LCD technology. [3] In addition, the transparency of TTFTs should offer improved back-lighting efficiency of TTFT-based LCDs over conventional amorphous silicon TFT LCDs.

Beyond providing a potential means to improving LCD technology, TTFTs open the door to transparent electronics. TTFTs, transparent capacitors, resistors, *etc.* could be imbedded into glass windshields of cars or windows in buildings. Perhaps the most intriguing implementation of transparent electronics is in a transparent display. TTFTs are a fundamental building-block of any active-matrix transparent display. Until now, transparent displays are primarily realized as camera tricks for Hollywood movies. The full implications of TTFT technology remains to be seen.

TTFT technology is still in its infancy and much work remains to be done. First, little is known about how best to process materials for TTFT manufacturing. Second, little is understood about the device physics of ZnO TTFTs, beyond that they possess transistor behavior. Finally, the reliability of ZnO TTFTs has not been explored.

A goal of this dissertation is to demonstrate a low-cost and efficient method for depositing thin-films useful for TTFT applications. Thus, low-cost deposition of body ZnO and gate insulators is of primary interest. It is possible to produce high-quality ZnO thin-films via liquid-phase deposition methods. The work presented in this dissertation constitutes the first demonstration of spin-coated ZnO TTFTs and spin-coated HfO_2 gate insulator ZnO TTFTs.

Spin-coating is an inherently low-cost and simple liquid-phase deposition method. Additionally, the chemicals required for spin-coating deposition of ZnO and HfO_2 are relatively inexpensive, environmentally benign, easy to prepare, and possess few health risks. Spin-coating deposition has a potentially much higher throughput than that of an equivalent vacuum deposition method. Also, the maintenance costs and purchase price of a spin-coating deposition system are significantly less than for an equivalent vacuum deposition system.

HfO_2 is of great interest as a high dielectric constant gate insulator for next-generation silicon CMOS technology, and it is also of interest for use in TTFTs. [4] HfO_2 is typically deposited via vacuum deposition methods. Very little effort has been devoted to liquid phase deposition of HfO_2. [5] In this dissertation, the electrical properties of spin-coated HfO_2 insulators are presented for the first time.

A method for processing ZnO TTFTs with photolithography is demonstrated in this dissertation. Patterning TTFTs via photolithography is essential to their eventual integration into LCDs and other integrated circuits. Additionally, small TTFTs defined by photolithography do not necessarily operate the same as larger devices constructed using shadow mask pattern definition. While shrinking TTFT device dimensions reduces parasitic capacitances, the current density at the source and drain greatly increases. Thus, source and drain resistance becomes increasingly

problematic as device dimensions shrink. TTFT scaling issues are explored in this dissertation.

The organization of this dissertation is as follows. Chapter 2 is a review of relevant literature and technical background. Chapter 3 provides a description of the processing and characterization methods used in this dissertation. Chapter 4 contains the results of spin-coated thin-film studies of ZnO, HfO_2, SrS, and MgS. Chapter 5 presents the electrical characteristics of ion-beam sputtered ZnO TTFTs, spin-coated ZnO TTFTs, and spin-coated HfO_2 gate ZnO TTFTs. Finally, Chapter 6 contains conclusions and recommendations for future work.

2. LITERATURE REVIEW AND BACKGROUND

2.1 Zinc Oxide Transparent Thin-Film Transistor

The first enhancement mode, *i.e.* the channel is off with zero volts on the gate, n-channel zinc oxide transparent thin-film transistor (TTFT) was developed by Hoffman *et al.* [1, 2] Generally, it is desirable that a transistor is enhancement-mode since it is simpler and often lower power is required when the off logic state of a transistor is zero volts on the gate. The Hoffman *et al.* transistor is a staggered, bottom-gate device with the source and drain on the top, as shown in Fig. 2.1. It is constructed on an indium tin oxide (ITO) and aluminum titanium oxide (ATO) coated glass substrate. The body is deposited through a shadow mask via ion-beam sputtering and annealed in oxygen at a nominal temperature of $700°C$. The source and drain are also deposited via ion-beam sputtering through a shadow mask. The Hoffman *et al.* transistor has a threshold voltage of 10 to 20 V, a channel mobility of 0.3 to 2.5 cm^2/Vs, and a drain current on-to-off ratio of 10^7.

Masuda *et al.* demonstrated a similar transparent ZnO transistor. [6] The Masuda *et al.* transistor consists of a 250 nm thick SiO_2 layer with a 50 nm cap of SiN_x as a gate insulator. The Masuda *et al.* transistor is a depletion-mode transistor, *i.e.* requires a negative gate voltage to turn off the channel, with poor saturation characteristics and a large "off" current leakage. The body ZnO is deposited by pulsed laser deposition.

A ZnO transistor is also demonstrated by Carcia *et al.* [7]. It is a staggered bottom-gate, with source and drain on top transistor, see Sec. 3.2.1.1. It is constructed on a Si substrate using a thermally grown SiO_2 gate insulator, a RF

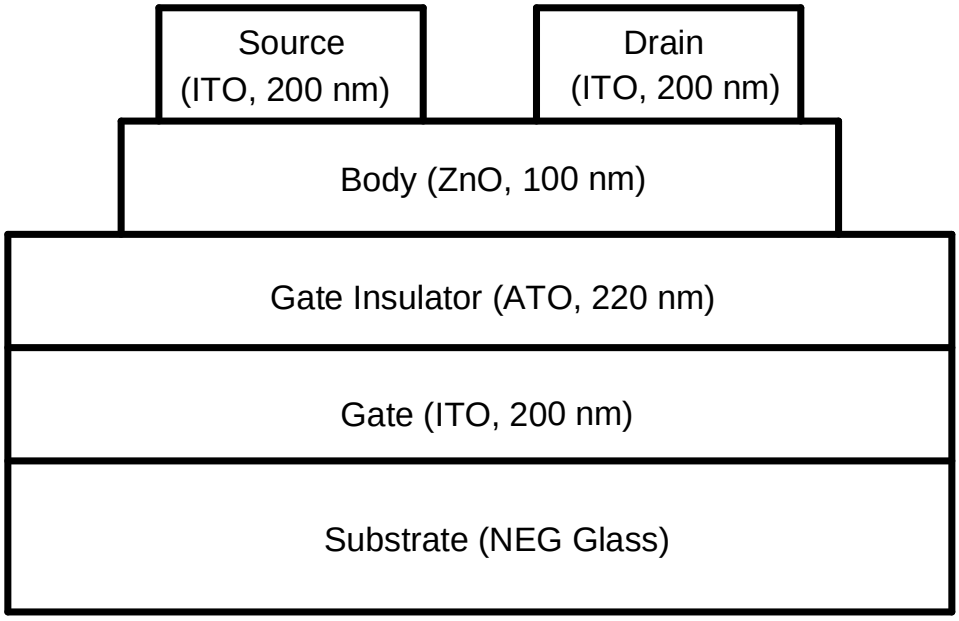

Figure 2.1: A diagram of the Hoffman *et al.* TTFT structure.

sputtered ZnO body, and Ti-Au source and drain contacts. Clearly this is not a transparent transistor since the substrate and source and drain regions are opaque. This result is of interest, however, since a drain current on-to-off ratio of 10^6 and a mobility of 2 cm^2/Vs are achieved from a ZnO body which is sputtered onto an unheated substrate with no post-deposition annealing. This result implies that ZnO TTFTs may be compatible with low-temperature plastic substrates.

European patent application 99972374.5 makes broad intellectual property claims with respect to a wide variety of transparent conductive body materials in a vast array of transistor implementations. [8] Very few, if any of these claims appear to have been reduced to practice. Data are given for a depletion-mode transistor with poor saturation characteristics. However, it is unclear if this is a characteristic curve from a truly transparent transistor or is simply from a transistor with a ZnO body.

Recently Nomura *et al.* demonstrated a high mobility ($\sim 80\ cm^2/Vs$) transparent transistor based on an $InGaO_3(ZnO)_5$ superlatice. [4] This work provides an existence proof that high mobility TTFTs are possible. However, the Nomura *et al.* TTFT requires the use of a single crystal body material deposited via pulsed laser deposition (PLD) and annealing at $1400°C$. Thus, the process proposed and the materials employed would be very expensive to manufacture. Interestingly, the Nomura *et al.* TTFT employs a HfO_2 gate which, they claim, results in a factor of ~ 40 improvement in channel mobility compared to an otherwise identical TTFT with an Al_2O_3 gate.

Nishii *et al.* constructed a ZnO thin-film transistor (TFT) using the same device structure as a commercial LCD TFTs. [3] The body ZnO is deposited by pulsed laser deposition and annealed at $300°C$. Nishii *et al.* observed field-effect mobilities as high as $7\ cm^2/Vs$. Additionally, they showed that the field-effect mobility is higher when a $CaHfO_x$ buffer layer is placed between the SiN gate insulator and the ZnO body.

ZnO TTFTs are typically compared to amorphous silicon and organic thin-film transistors (TFT) since the applications may be similar. Typical amorphous silicon TFT mobilities are 0.5 to 1 cm^2/Vs and the theoretical limit is estimated to be $\sim 10\ cm^2/Vs$. [9] The largest organic TFT mobility reported is 2.7 cm^2/Vs for pentacene which is approaching the theoretical limit of 10 cm^2/Vs for organic TFTs. [10]

2.2 TTFT Processing and Integration

Since the TTFT is a relatively new invention, a comprehensive discussion of previously utilized processing and integration methods is quite short. The pat-

terning methodologies discussed below are primarily used in silicon semiconductor technology, with the exception of shadow masking. The ZnO processing techniques developed in this dissertation leverage off of these existing methodologies.

2.2.1 Shadow Mask

The initial TTFT development was accomplished via deposition of thin-films through a shadow mask, *i.e.* a thin metal plate with holes cut where a thin-film is to be deposited. [1, 2] Shadow masking allows thin-films to be patterned quickly and easily and it is an essential development tool. However, shadow masking has many disadvantages. First, the thickness of the shadow mask limits the minimum critical dimension possible since shadow masked features must be much larger than the mask thickness for all but a normally-directed deposition. In addition, a shadow mask must be mounted with the substrate in the deposition chamber, thus limiting the alignment tolerance to that obtainable via visual hand alignment. Finally, the contact between the shadow mask and the substrate is a potential source of scratches and particles. Thus, shadow masking becomes increasingly difficult and expensive for critical dimensions less than $\sim 0.5\ mm$. Due to the large critical dimensions TTFTs made via shadow masking are inherently slow, as discussed in Sec. 3.3.1.

2.2.2 Photolithography

Photolithography is the basic method used for patterning associated with thin-film deposition, implantation, diffusion, *etc.*, in integrated circuit manufacturing. Currently, highly sophisticated photolithography tools are capable of reproducibly and reliably defining and aligning critical dimensions as small as 90 nm, and this dimension is constantly shrinking. Photolithography is the most readily available

method for defining small dimensions. Section 3.2.7 discusses how photolithography is adapted to TTFT processing.

Photolithography consists of coating (typically spin-coating) the area to be patterned with a photo-sensitive polymer called photoresist, and exposing selected areas to ultraviolet light through a mask. Positive photoresist becomes soluble in a developer solution upon exposure to UV light and negative photoresist is rendered insoluble in a developer solution upon exposure to UV light. The photoresist is then developed in a developer bath in which the soluble material is removed. The remaining photoresist may then be used to pattern a thin-film. A diagram of the photolithography process is shown in Fig. 2.2. Since many excellent text books covering photolithography in detail are available, a detailed description of the photolithography literature is not included here. [11, 12]

2.2.2.1 Lift-Off

Lift-off is a patterning method often employed when etching is not an option, either due to process incompatibility or the lack of a suitable etch method. For example, in GaAs technology a gold lift-off process is often used since gold is relatively inert and extremely hazardous chemicals are required to etch it. Lift-off is also useful during process development when it is uncertain how the etch chemistry will affect other thin-films or if an etch recipe has not yet been developed. It is, in principle the simplest photolithography patterning method, but it is often troublesome to successfully accomplish.

Lift-off consists of depositing a thin-film to be patterned on top of a patterned photoresist layer. [11, 12, 13] A diagram of the lift-off process and typical problems encountered are shown in Fig. 2.3. After film deposition, the photoresist is removed

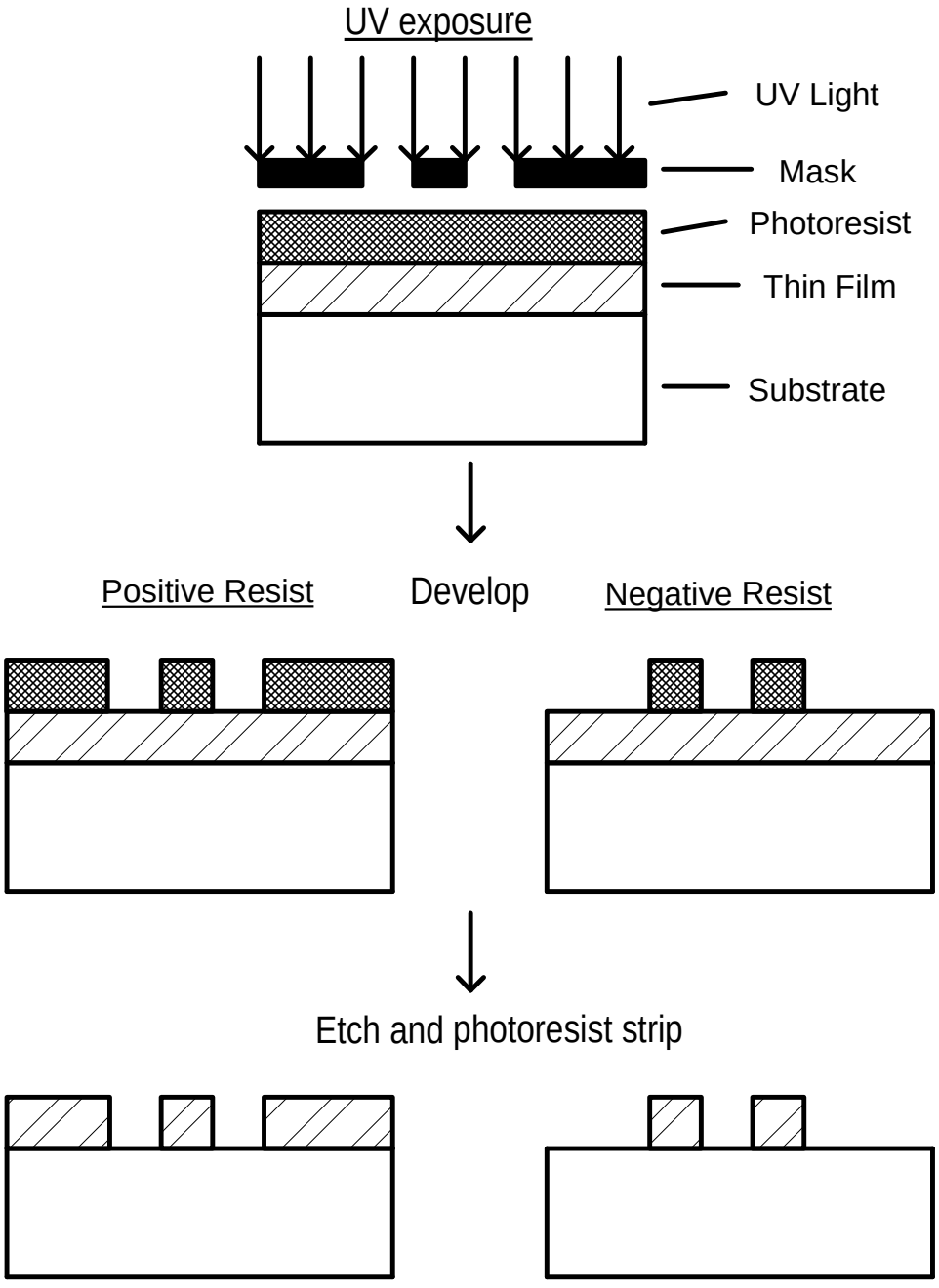

Figure 2.2: A photolithography process for patterning using positive or negative photoresist.

and, ideally, the film on top of tge photoresist is removed with the photoresist, while the film remains in the areas not covered by photoresist. In practice, however, the thin-film often does not break off or detach at the edge of the photoresist, so that a spire or hanger remains, as shown in 2.3. Lift-off may be employed with highly conformal depositions but often a photoresist overhang must be created to aid in lift-off. Thus, lift-off is best suited to patterning of normally-directed depositions. [13] In addition, the thin-film deposition process used must be compatible with the photoresist. Typically photoresist is limited to a maximum temperature of $\sim 200°C$. Also, some gas plasmas, *e.g.* oxygen, damage photoresist.

2.2.2.2 Etching

Etching is typically used to remove undesired areas of a thin-film. Thin-film areas are first masked off with photoresist and then the unprotected areas are removed with an etchant. Etching avoids many of the problems associated with lift-off, *e.g.* spires, hangers, and photoresist damage during film deposition. However, an etch chemistry must be tailored to and optimized for a specific thin-film material and often a specific method of thin-film deposition. Etch rates often vary from one thin-film of the same material to the next if the deposition method or process recipe is changed. In addition, if multiple thin-film layers, *e.g.* Ti and Au, are to be removed with one mask step a separate etch must often be used for each material. Conversely, if the etch is not selective, *i.e.* only etches the desired thin-film layer, material other than that desired to be etched may also be removed.

Etching may be divided into two general types, wet and dry. [11, 12, 14] With wet etching, the substrate is dipped in a liquid solution that is chosen to attack the thin-film at a controlled rate. Typically, wet etches are isotropic but anisotropic wet

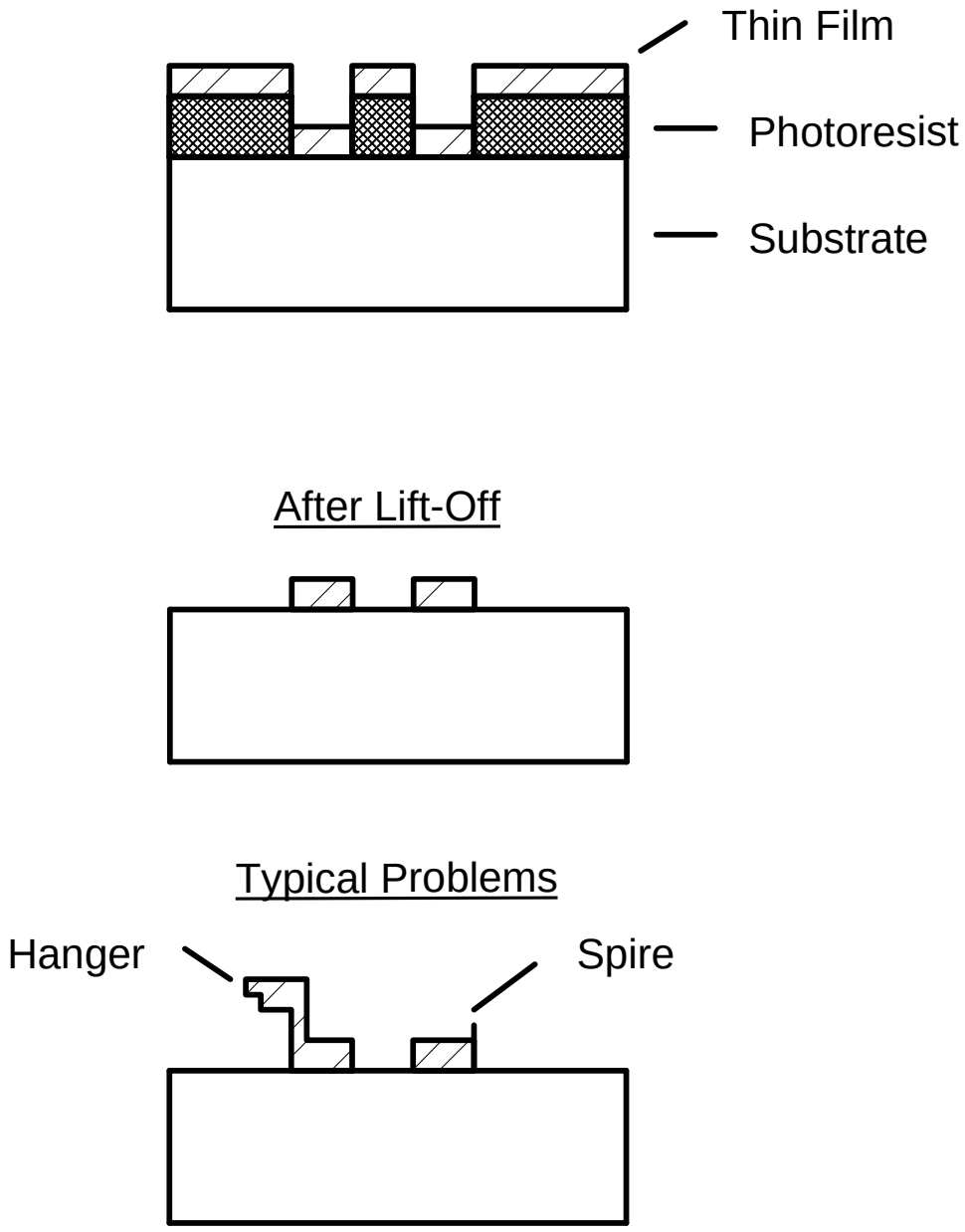

Figure 2.3: A diagram of the lift-off process and typical problems associated with lift off.

etches do exist for highly crystalline materials, *e.g.* KOH for crystalline Si. Because of isotropic etching, deep trenches often become severely undercut. In addition, relatively inert and stable thin-films often require the use of extremely toxic and corrosive chemicals, *e.g.* SiO_2 requires an HF wet etch.

Dry etching is generally accomplished by exposing the film to be etched to a plasma-activated reactive gas. Dry etching is a combination of a chemical attack of the surface in conjunction with physical ion bombardment, *i.e.* sputtering, of the thin-film. Dry plasma etching is inherently anisotropic, which leads to a reduction or elimination of undercutting. However, dry etching must be tailored to specific thin-film chemistry and dry etch processes are not always available for new or exotic materials.

2.3 thin-film Deposition Overview

For the purposes of this dissertation thin-film deposition methods may be divided into two general groups: vacuum and non-vacuum deposition methods. Although the work presented in this dissertation primarily focusses on a non-vacuum method, liquid phase deposition via spin-coating, vacuum deposition methods are surveyed for comparative purposes.

2.3.1 Vacuum Deposition Methods

Vacuum deposition techniques generally involve some kind of sealed metal chamber (typically stainless steel) pumped with both a roughing and a high vacuum pump. The roughing pump is typically a rotary vane pump and the high vacuum pump is a cryogenic, diffusion, or turbomolecular pump. The major drawback of

vacuum deposition is the expense of maintaining and operating the pump stack and vacuum chamber. In addition, throughput, *i.e.* the number of depositions per unit time, is limited by the pumping speed. However, the cleanliness and the extremely low pressure of a vacuum system are ideal conditions for high quality thin-film growth.

2.3.1.1 Evaporation

Thermal evaporation is the simplest vacuum deposition method. [11, 12] Thermal evaporation is accomplished by heating a material source with a resistive heater to its evaporation or sublimation temperature so that material is ejected thermally from the source material surface. The resulting material condenses onto the first relatively cold surface encountered and thus, builds up on a substrate placed within a line of sight of the thermal source. High vacuum is required to maintain a large mean free path of ejected material. Typically, the substrate is placed as far away from the source as practical and a planetary system is often employed, to improve film uniformity.

Thermal evaporation is not suitable for evaporation of refractory materials since the maximum source temperature is limited to the melting or sublimation temperature of the heater. Therefore, refractory materials require the use of an electron beam. A directed electron beam is capable of locally heating source material to extremely high temperatures. However, the source material must be pressed into a dense pellet free of voids so that the temperature gradients produced by an electron beam do not explode the pellet. A similar material preparation is not required for thermal evaporation since the stress placed on the source material is not as great.

A major drawback of evaporation is that the stoichiometry is not necessarily preserved from source material to thin-film. Thus, it is difficult to produce binary, ternary, and higher order compounds of a controlled stoichiometry without first performing an empirical study of source material composition versus thin-film composition. Material development with evaporation is thus limited.

2.3.1.2 Sputtering

Sputtering is a useful and widespread method of producing thin-films of a controlled stoichiometry. [11, 12] There are many variations of the basic sputtering process. Fundamentally, sputtering consists of bombarding a target, *i.e.* source material, with high energy ionized species. The resulting physical impact frees some target material and imparts kinetic energy. Some of the removed target material comes to rest on a nearby substrate and thus a thin-film grows.

A common method of generating the high bombardment energy species necessary for sputtering is via a radio frequency (RF) or direct current (DC) plasma. Typically, RF sputtering is more common since it eliminates the DC problem of a static charge build up on the target. Often magnetic fields created by permanent magnets or electromagnets embedded in the sputtering source are employed to aid in confinement of electrons near to the target surface and to increase the density of electrons responsible for causing ionizing collisions. Sputtering using an embedded permanent magnet in the sputtering gun is referred to as magnetron sputtering. Sputtering offers a great degree of process control since the plasma power, sputtering gas, pressure, flow rate, and target-to-substrate distance may be separately controlled.

The sputtering method employed in this dissertation is referred to as ion-beam sputtering, as shown in Fig. 2.4. Ion-beam sputtering consists of generating an ion-beam and directing it at a target material. Ion-beam sputtering has the advantage of removing high energy particle generation away from the target so that less stress is placed on the target. Also, targets and substrates may quickly be changed without the use of a load lock. Typically the deposition rate is controlled by the beam current; larger beam current results in a higher sputtering rate.

2.3.1.3 Pulsed Laser Deposition (PLD)

Pulsed laser deposition (PLD) is a method for depositing thin-films involving the use of laser ablation of a target source. The resulting ablation plume deposits on to a nearby substrate. A primary advantage of this method is that a wide variety of materials may be simply deposited and that the film composition tends to closely resemble the target composition. However, PLD is not suitable for high-volume manufacturing since it involves the use of an expensive tool in terms of purchase price and maintenance.

2.3.1.4 Chemical Vapor Deposition (CVD)

H. O. Pierson defines chemical vapor deposition (CVD) as a "deposition of a solid on a heated surface from a chemical reaction in the vapor phase." [15] This general definition includes a wide variety CVD variants including atmospheric pressure CVD. However, since the majority of CVD reactors and the CVD systems of interest in this dissertation require vacuum stacks, CVD is classified as a vacuum deposition method for the purposes of this dissertation. Plasma-enhanced CVD

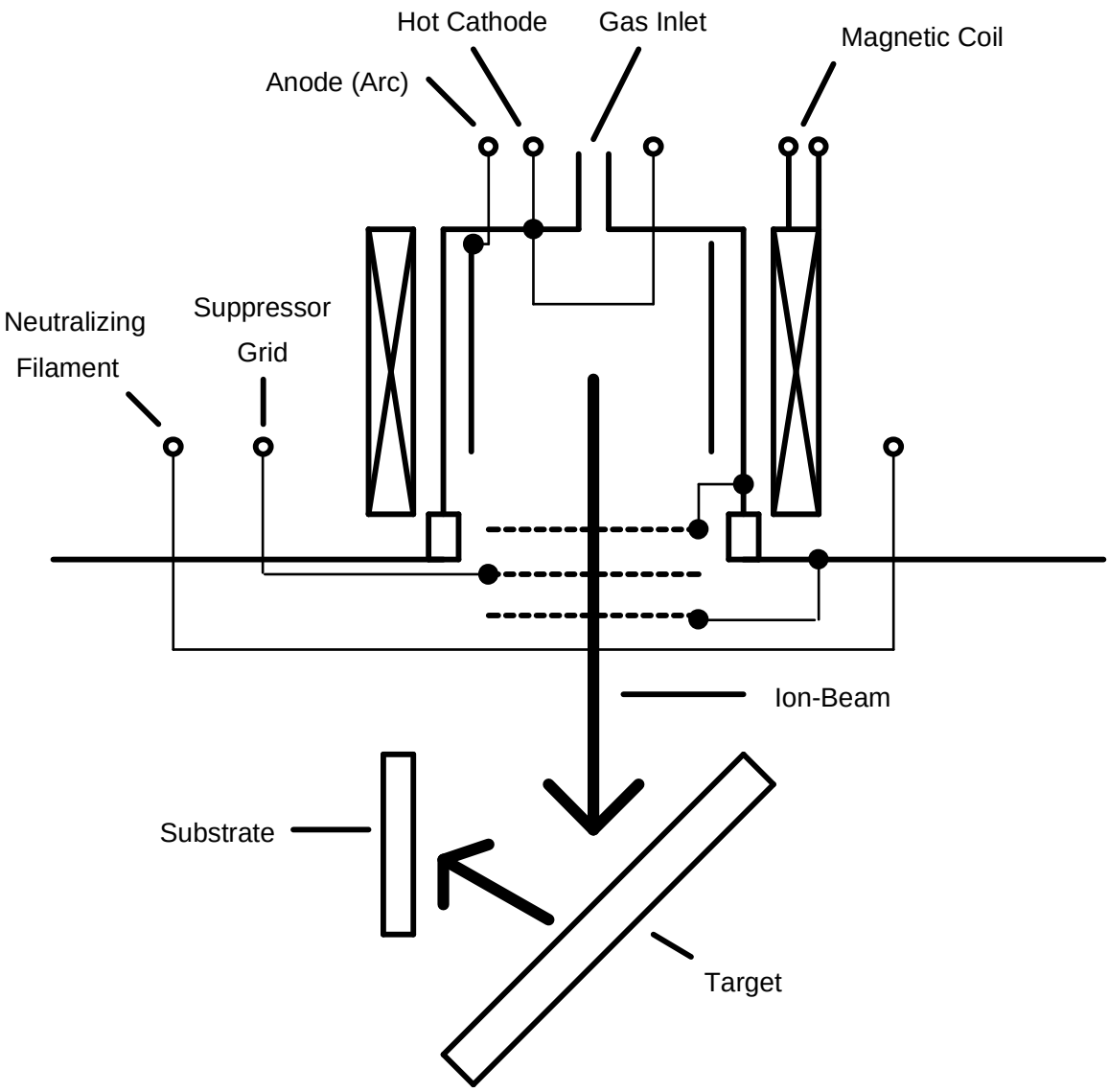

Figure 2.4: A schematic of a typical ion-beam sputtering system. Notice that the lower part of the schematic is within the high vacuum chamber and the upper part is outside. A glow discharge is generated between the anode and cathode. An ion-beam is accelerated into a target and the resulting sputtered material builds up on the substrate.

(PECVD) and metal-organic CVD (MOCVD) are of primary interest here. For an explanation of other CVD methods see the references listed. [11, 12, 14, 15]

PECVD is a CVD process that uses a plasma to activate the gas species and enhance deposition. PECVD reactors normally operate at fairly low temperatures ($\approx 300°C$), produce good step coverage, and have a high deposition rate. However, particle and chemical contamination is often a problem. [11] In this dissertation PECVD is used to deposit SiO_2 for gate insulators and passivation layers. In addition, PECVD may be use for ZnO deposition. [16] For a thorough discussion of PECVD deposition of SiO_2, see Appendix B.

MOCVD involves the use of uses a metal-organic vapor as a metal source, *e.g.* dimethyl zinc. MOCVD reactions typically occur at pressures from 1 Torr to atmospheric pressure and temperatures from 300–800$°C$. Abrupt interfaces (1 nm) and film thicknesses less than 10 nm may be produced with a high-quality MOCVD system. However, MOCVD systems are expensive and operating costs are high. [15]

2.3.2 Non-Vacuum Deposition Methods

Non-vacuum thin-film deposition methods have the obvious advantage of the elimination of the costly pumping stack and vacuum chamber associated with vacuum deposition methods. Additionally, tool throughput is not limited by the pumping speed of the vacuum stack. However, often the liquid or vapor deposition environment of non-vacuum methods is less than ideal for high-quality thin-film crystal growth.

The focus of the work presented in this dissertation is ZnO deposition via spin-coating. Spin-coating deposition is related to sol-gel based deposition techniques. [17, 18, 19] A sol-gel, according to its most general definition, is a "colloidal route

used to synthesize ceramics with an intermediate stage including a sol and/or a gel state." [18] Since the precursor used in the spin-coating of ZnO is not colloidal, it cannot be considered to be a sol-gel process, at least by a strict definition of the term. Thus, the more general designation "liquid-phase deposition method" is used throughout this dissertation instead of the term sol-gel. However, it should be noted that many researchers incorrectly use the term sol-gel to refer to all liquid-phase deposition methods.

There are three general methods used to accomplish liquid-phase deposition: dip coating, spin-coating, and spray pyrolysis. The simplest liquid-phase deposition method is dip coating. Dip coating involves simply dipping a substrate into a resin bath and then slowly pulling the substrate out. [20, 21] As the substrate is pulled out of the dip, the excess resin runs off the substrate into the dip and then the solvent evaporates, leaving behind a thin-film. Often the dip is repeated multiple times in order to build up a thicker film. Dip coating is perhaps the oldest method of thin-film deposition known. It is difficult to say when the first human dipped a piece of jewelry or pottery in a bowl of paint.

Spin-coating consists of placing a small amount of liquid spin resin onto a substrate to be coated. The substrate is then spun up to speeds of typically 3000–4000 rpm. As the substrate spins, the resin spreads across the substrate and the solvent begins to evaporate. Once a majority of the solvent has evaporated a thin-film remains. The substrate is typically then "soft baked" at a low temperature ($\sim 100°C$) to remove any remaining solvent. Spin-coated film thickness is primarily controlled by the spin speed, resin viscosity, solvent volatility, and spin time. [22, 23]

Finally, the most sophisticated of these liquid-phase deposition methods is spray pyrolysis. [18, 24] With spray pyrolysis a solution is sprayed at a heated substrate. When the spray droplets hit the substrate, the desired solute condenses

onto the substrate while the solvent evaporates off. Over time a thin-film builds up on the surface.

2.4 Zinc Oxide Deposition Methods

When investigating the properties of a new method of film deposition it is important to keep in mind the thin-film properties that are truly materials properties and those that are related to the deposition method. A large variation in film resistivity, *i.e.* insulating to $\sim$ 100 $\mu\Omega$-cm, is observed with ZnO thin-films, depending on dopant type and concentration, as well as on processing conditions. Additionally, annealing can greatly influence film conductivity. Generally, annealing in a reducing atmosphere, *e.g.* hydrogen, vacuum, *etc.*, increases the conductivity by creating oxygen vacancies, whereas annealing in an oxidizing atmosphere, *e.g.* oxygen, decreases the conductivity. [24]

ZnO possesses the wurtzite crystal structure and tends to crystallize fairly easily so that most ZnO thin-films are polycrystalline. [25] Also, most methods of depositing ZnO produce films oriented along the (002) plane relative to the substrate.

2.4.1 Zinc Oxide Deposition Via Sputtering

RF magnetron sputtering is widely used for the deposition of ZnO. [26, 27, 28, 29] The work of A. V. Singh *et al.* is of particular interest since they show that oxygen partial pressure is inversely proportional to the degree of (002) crystal orientation. [28] However, the data presented is from ZnO codoped with GaN so that it is not clear if this is a general trend applicable to all ZnO thin-films.

Ion-beam and reactive sputtering have also been explored for the deposition of ZnO. [30, 31, 32, 33, 34] The work of Y. Qu *et al*. shows that crystal orientation of ion-beam sputtered ZnO improves as the substrate temperature during deposition is increased up to approximately $250°C$. [32] W. Li *et al*. report that the carrier concentration is inversely proportional to annealing temperature and that the Hall mobility is proportional to annealing temperature. [33] These trends are attributed to improvements in crystallinity.

Ion-beam-assisted reactive deposition has also been used for the deposition of high-quality ZnO. [35, 36] Technically, this is not a sputter deposition method but it is related since an ion-beam is involved. S. Whangbo *et al.* produced high quality (002) oriented ZnO via this method. [36] D. H. Zhang *et al.* demonstrate that ZnO crystallinity and stoichiometry greatly improves upon annealing above $500°C$. [35]

2.4.2 Zinc Oxide Deposition Via Pulsed Laser Deposition (PLD)

PLD is well suited to producing thin-films in laboratory conditions. Thus, ZnO films produced via PLD are typically high quality and highly (002)-oriented with the application of substrate heat during deposition. [37, 38, 39, 40] Additionally, T. Nakamura *et al.* are able to achieve (0001)-orientated ZnO thin-films by using a cubic (111) $(LaAlO_3)_{0.3}(SrAl_{0.5}Ta_{0.5}O_3)_{0.7}$ substrate. [41]

2.4.3 Zinc Oxide Deposition Via Chemical Vapor Deposition (CVD)

A few different ZnO MOCVD recipes have been proposed and investigated. [16, 42, 43, 44, 45, 46] O. F. Khan *et al*. first proposed the use of zinc acetate

as an MOCVD precursor. [42] Unfortunately they did not include much thin-film characterization data in their reports; thus, it is difficult to assess the quality of their ZnO thin-films. However, Gruber *et al.* achieved oriented ZnO via MOCVD. [43] The Gruber *et al.* recipe uses diethylzinc [DEZn ($(C_2H_5)_2Zn$)] as their zinc precursor. [43]

ZnO via PECVD is of particular interest since Oregon State University has a PECVD and this method may prove to be viable for high volume ZnO manufacturing. Li *et al.* propose a simple and straightforward method for depositing ZnO via PECVD using $Zn(C_2H_5)_2$ and carbon dioxide (CO_2) as the oxygen source. [16] They achieved very high quality (002)-oriented ZnO films.

2.4.4 Zinc Oxide Deposition Via Liquid Phase Methods

Initial investigation of ZnO deposition using a liquid phase method was accomplished by Spanhel *et al.* [47, 48]. This work introduced the use of zinc acetate as a ZnO precursor. Zinc acetate based precursors have been employed in most subsequent ZnO liquid-phase deposition. This early work primarily focused on chemical synthesis and chemical properties of the solution; very little attention was devoted to the thin-film properties.

W. Tang *et al.*, T. Tsuchiya *et al.* and Y. Ohya *et al.* were the first to focus on the thin-film properties of ZnO produced from a zinc acetate based solution. [49, 50, 51] All three of these works report on the properties of aluminum-doped ZnO. W. Tang *et al.* investigated the optimum doping concentration and annealing temperature. T. Tsuchiya *et al.* utilized XRD, XPS and SEM to characterize ZnO properties as a function of variation in process parameters. A series of papers

followed on ZnO deposition using zinc acetate, all of which use similar solutions yielding similar results. [52, 53, 54, 55, 56, 57]

The work of Y. Ohya *et al.* is of greatest interest since they are the first group to show that highly oriented ZnO could be produced from a liquid phase method. [51] They assert that the degree of crystal orientation depends on the concentration of the spin solution and the temperature of the post-deposition heat treatment. A large number of papers appeared after publication of this Y. Ohya *et al.* paper. [58, 59, 60, 61, 62, 63, 64, 65] Papers by M. Ohyama *et al.* and J. H. Lee *et al.* stand out as particularly significant and relevant. [60, 65] M. Ohyama *et al.* provide a model explaining grain growth and crystal orientation as a function of film thickness. J.-H. Lee *et al.* examine a large variety of annealing treatments and their effect on ZnO film quality and orientation. They show that the initial solvent bake temperature strongly affects the film orientation. Films initially fired at a temperatures above $350°C$ show the highest degree of crystal orientation.

The vast majority of the research reviewed here focuses on ZnO from zinc acetate-based spin solutions. The only exceptions are papers by T. Tsuchiya *et al.* and B. Wessler *et al.* [50, 64] T. Tsuchiya *et al.* present a comparison of thin-films from an acetate and a nitrate-based solution. They conclude that the acetate-based solution produces a higher conductivity ZnO thin-film than the nitrate-based solution since at the high temperature ($900°C$) required to anneal their nitrate-based ZnO thin-film there is significant interaction between the thin-film and the substrate. It is, thus, unclear if this conclusion is based on thin-film properties or the softening temperature of the substrate used. This work leaves more questions than answers since key pieces of data are strangely left out of the paper, *i.e.* the substrate used, conductivity versus annealing temperature, and film thickness. Thus, it is difficult for the reader to follow the reasoning leading to the conclusions given. Also, it

should be noted that the zinc nitrate solution, *i.e.* a water, zinc nitrate, ethylene glycol, and glycerol mixture, used in this study is distinctly different than the zinc nitrate solution discussed in this dissertation, *i.e.* a water, zinc nitrate, and glycine mixture.

B. Wessler *et al.* explored the use of zinc nitrate, zinc acetate, zinc formate, and zinc-2-ethylhexanoate in combination with an array of solvents and complexing agents, *i.e.* stabilizers or/and thickenners. [64] They assert, without presenting any real data, that zinc-acetate and ethanolamine in a solvent of 2-methoxyethanol produce oriented films, but that the other solutions investigated are not effective. This is inconsistent with other papers in which oriented films are produced from many different types of zinc acetate solutions. [62, 63] B. Wessler *et al.* make no mention of attempting to use glycine as complexing agent, as is done with the zinc nitrate based spin solutions of this dissertation.

There appears to have been no significant published data attempting to optimize spin solutions based on any ZnO precursors other than zinc acetate. As a consequence, it seems that many researchers have assumed that zinc acetate is the optimal spin solution precursor for depositing ZnO thin-films. The data presented in Chapter 4, however, indicates that the quality of spin deposited thin-films, not surprisingly, varies widely with processing conditions. Additionally, optimal processing conditions for one spin solution chemistry are not necessarily optimal for all other spin solution chemistries. Thus, it makes little sense to deposit many thin-films from different spin solution chemistries using the same processing conditions and to conclude that the best solution chemistry yields the best thin-film. Unfortunately, it seems that it is this logic that has led researchers away from trying new solution chemistries for the liquid phase deposition of ZnO.

Spray pyrolysis is closely related to spin-coating and dip coating deposition in that the precursor solutions tend to be similar. Studenikin *et al.* use a zinc nitrate spray solution to achieve (002)-oriented ZnO. [66] Additionally, Paraguay *et al.* obtain similar results using a zinc acetate precursor. [67]

2.5 Insulators

Gate insulators and eventually inter-layer dielectrics are important constituents of a viable commercial TTFT technology. Furthermore, gate insulator performance is critical to TTFT performance. Current versions of TTFTs produced at Oregon State University utilize ATO, an aluminum oxide and titanium oxide superlattice, as an insulator, as it is very well suited for TTFT use. However, it is a Planar proprietary insulator that cannot be produced at Oregon State University. In addition, the dielectric constant is not as large as that found in high-k dielectrics. Thus, other gate insulator possibilities should be considered.

Table 2.1 is list of possible TTFT insulators, including important device parameters. The relative dielectric constant (κ) is a measure of how effective the insulator is at polarizing with respect to the application of an electric field. The bandgap (E_g) is a measure of the energy gap between the conduction and the valence band. The electron affinity (χ) is measured from the bottom of the conduction band to the vacuum level. The conduction band offset (ΔE_c) is the offset between the conduction band of ZnO and the conduction band of the insulator. ΔE_c is calculated by subtracting the χ of the insulator from the χ of ZnO. The valence band offset (ΔE_v) is the offset between the valence band of ZnO and the valence band of the insulator. ΔE_v is calculated by subtracting $\chi + E_g$ of ZnO from $\chi + E_g$ of the

insulator. Negative ΔE_v values indicate a barrier in which holes gain kinetic energy when passing from ZnO to the insulator, *i.e.* it is not an effective hole barrier.

A large dielectric constant is desirable since this results in more induced channel charge (Q_{ch}) for a given gate overvoltage, *i.e.* the gate voltage in excess of the threshold voltage. Q_{ch} is calculated by

$$Q_{ch} \approx C_i(V_{GS} - V_T), \tag{2.1}$$

where V_{GS} is the gate to source voltage, V_T is the threshold voltage, and C_i is the insulator capacitance. A larger Q_{ch} yields a larger TTFT drive current. The insulator capacitance per unit area is given by

$$C_i = \frac{\kappa\epsilon_0}{d}, \tag{2.2}$$

where ϵ_0 is the permittivity of free space, and d is the gate insulator thickness. Equation 2.2 indicates that C_i may be increased by decreasing d. Since d is simply a device dimension, it is evident from Eq. 2.2 that the the only materials parameter that can increase the insulator capacitance is κ.

High gate leakage through the insulator results in poor on-to-off performance and in extreme cases the inability to form a channel. Generally, the wider the band gap of an insulator, the lower the expected leakage current. Additionally, the conduction and valence band offset for a specific material may help to predict insulator performance for a given semiconductor material. The conduction (valence) band offset is the difference in energy between the insulator conduction (valence) band and the semiconductor conduction (valence) band. A large conduction (valence) band discontinuity is desirable in order to minimize electron (hole) injection and concomitant conduction in the insulator. Thus, it is desirable that the conduction and valence band offsets are as large as possible, generally $> 1\ eV$.

Table 2.1: Important TTFT gate insulator properties. κ is the dielectric constant, E_g is the bandgap, χ is the electron affinity, ΔE_c is the conduction band offset to ZnO, and ΔE_v is the valence band offset to ZnO.

Insulator	κ	E_g (eV)	χ (eV)	ΔE_c (eV)	ΔE_v (eV)	References
ZnO		3.2–3.3	4.5–5	N/A	N/A	[24]
SiO_2	3.9	8.9–9	0.9	4.1–3.6	1.5–2.2	[68, 69, 70]
Si_3N_4	7–7.5	5–5.3	2.1	2.4–2.9	-1.2– -0.3	[68, 69, 70]
ATO	11–18	Al_2O_3 & TiO	-	-	-	[71]
Al_2O_3	9	8.7–8.8	∼1	∼3.5–4	∼1.4–2.1	[69, 70, 72]
$BaTa_2O_6$	20–30	-	-	-	-	[73, 74]
HfO_2	25	5.7–6	∼2.5	∼2–2.5	∼-0.1–0.8	[69, 70, 72]
TiO_2	80	3.05–3.5	∼3.9	∼0.6–1.1	∼-1.35– -0.3	[69, 70]
Y_2O_3	15	5.6–6	∼2	∼2.5–3	∼-0.7–0.3	[69, 70]
La_2O_3	30	4.3–6	∼2	∼2.5–3	∼-2–0.3	[69, 70, 72]
Ta_2O_5	26	4.4–4.5	3.3–3.2	1.2–1.8	-1.7–0.1	[69, 70, 72]
ZrO_2	25	5.8–7.8	∼2.5	∼2–2.5	∼0–2.6	[69, 70, 72]

Two other important gate insulator considerations are process compatibility and electrical stability. The insulator deposition method and annealing requirement should be compatible with the glass substrate, ITO, and ZnO. The interface between the insulator and body should ideally be trap-free. Mobile ions, trapped charge, fixed charge, and interface trapped charge result in threshold voltage instabilities and they should be avoided whenever possible. [68] However, process compatibility and electrical stability are often difficult to predict and are often established empirically.

Notice that the conduction band offset between ZnO and a given insulator for all of the insulators considered in Table 2.1 are large, except for TiO_2. Thus, with the exception of TiO_2, leakage due to electron injection from the ZnO is likely to be small. However, for many of the insulators considered, ΔE_v is small or negative so that hole injection from the ZnO is possible, if holes are present in the ZnO. Since current-art ZnO TTFTs are exclusively n-channel devices, hole injection is not likely to be an issue unless holes are photogenerated by above bandgap UV absorption in the ZnO. If such photogenerated holes are present in a TTFT structure, their presence could give rise to various kinds of device instabilities associated with carrier transport and trapping in the ZnO and/or insulator if the valence band discontinuity is sufficiently small to allow for hole injection.

ATO, Al_2O_3, and SiO_2 and possibly ZrO_2, BTO, and HfO_2 appear to be the most attractive insulator candidates for TTFT applications when simply considering band offset issues with respect to ZnO. However, given the band offset and dielectric constant considerations, ZrO_2 and HfO_2 appear to be especially attractive choices as candidate materials for TTFT gate insulators. Additionally, Sviridova *et al.* and Nishide *et al.* demonstrated a viable method for spin-coating HfO_2. [5, 75] J.J. Yu *et al.* used UV irradiation of spin-coated HfO_2 to improve the stoichiometry of the resulting HfO_2. [76]

2.6 Transparent Conductors

Transparent conductors are a fundamental building bock of TTFT technology. Transparent conductors make up the gate, source, drain, and eventually the interconnects. Transparent conductors generally consist of wide band gap (3.1 eV) semiconductors heavily doped so that the carrier concentration is large. This classification includes a wide range of possible materials. At this time the most relevant transparent conductors for TTFT technology are believed to be doped ZnO and ITO, see Table 2.2.

Generally a good transparent conductor has a low resistivity and a large optical transparency. Additionally, for TTFT applications the TTFT must form an injecting contact with the body material and must be process-compatible. Depending on the dopants and deposition methods used, resistivity can vary widely but ~ 100 $\mu\Omega$-cm is considered to be a high conductivity. Transparency is typically in the range of 80–90% in the visible portion of the electromagnetic spectrum for the transparent conductors considered here. For the case of the ZnO TTFT considered in this dissertation, ITO is known to form a good injecting contact to ZnO. [1, 2] Doped ZnO is expected to form an injecting contact to undoped ZnO.

Table 2.2 is a compilation of processing methods, possible dopants, and resistivity for some transparent conductors. Notice that the resistivity varies greatly depending on the deposition method employed. Also, liquid phase deposition of transparent conductors such as ITO and ZnO are demonstrated, resulting in thin-film properties of comparable quality to that obtained via traditional vacuum deposition methods. This indicates that liquid phase deposition methods may be a viable alternative to vacuum deposition methods.

Table 2.2: Electrical properties of transparent conductors and deposition methods employed.

Material	Deposition	Bandgap (eV)	Resistivity ($\mu\Omega$-cm)	References
Al	-	-	2.6	[77]
W	-	-	5.3	[77]
ITO	RF Sputtering	3–4.6	68	[24, 78]
ITO	dip-coating	3–4.6	800	[24, 79]
ITO	Spray Pyrolysis	3–4.6	100	[24]
ZnO:Al	RF Sputtering	3.1–3.6	200	[24, 26]
ZnO:Al	dip-coating	3.1–3.6	150	[24, 57]
ZnO:Al	CVD	3.1–3.6	240	[24, 80]
ZnO:Ga	RF Sputtering	3.1–3.6	~ 500	[24, 81]
ZnO:Ga	CVD	3.1–3.6	240	[24, 82]
ZnO:B	DC Sputtering	3.1–3.6	400	[24, 83]
ZnO:F	CVD	3.1–3.6	400	[24, 84]
ZnO:F	Spray Pyrolysis	3.1–3.6	6700	[24, 85]
ZnO:In	RF Sputtering	3.1–3.6	300	[24, 86]
ZnO:In	Spray Pyrolysis	3.1–3.6	1000	[24]
SnO_2:F	Spray Pyrolysis	3.7–4.6	100–1000	[24, 87]
SnO_2:Sb	Spray Pyrolysis	3.7–4.6	1000	[24]
SnO_2:F	Sputtering	3.7–4.6	2000	[24]
SnO_2:As	CVD	3.7–4.6	160	[24]
In_2O_3	Spray Pyrolysis	3.5–3.75	160	[24]
In_2O_3	Sputtering	3.5–3.75	330	[24]
In_2O_3:F	CVD	3.5–3.75	285	[24]
Cd_2SnO_4	Sputtering	2.7–3	130	[24, 88]

Many transparent conductors, *e.g.* ZnO, SnO_2, and Cd_2SnO_4, have resistivities that depend nonlinearly on film thickness, resulting in thin-films less than $\sim 100\ nm$ have much larger resistivities than expected from simple thickness scaling. [24, 26, 61, 81, 82, 85] This behavior is most pronounced for ZnO and SnO_2 thin-films. This thickness-dependent resistivity behavior is found to occur for ZnO thin-films which are doped with many different kinds of dopants, *e.g.* F, Al, and Ga, and which are deposited by many different methods, *e.g.* RF sputtering, CVD, dip coating, and spray pyrolysis. Thus, this nonlinear dependence of resistivity on thickness may be assumed to be a fundamental property of ZnO thin-films. However, a nonlinear dependence of resistivity on thickness is not a property of all transparent conductors, since it is not observed with ITO thin-films. [24, 79, 89] Hu *et al.* and Minami *et al.* attribute this behavior in ZnO to increased grain boundary scattering as the film thickness is reduced. [26, 82] However, neither Hu *et al.* nor Minami *et al.* offer compelling evidence to support this claim, and the results of this dissertation do not support this hypothesis either, as discussed in Sec. 6.2.2.4.

2.7 TTFT Device Physics

2.7.1 ZnO Electrical Properties

ZnO is well known to exhibit persistent photoconductivity (PPC). [90, 91] PPC depends strongly on annealing conditions and the ambient atmosphere. It is thought that PPC in ZnO is associated with chemisorption and desorption of oxygen on the ZnO surface. Chemisorbed oxygen depletes the ZnO surface because a conduction band electron is trapped at the ZnO surface, thereby mediating a transformation from physisorbed to chemisorbed surface oxygen. When the partial

pressure of oxygen is low and/or the surface is exposed to UV light, oxygen desorbs from the surface and the carrier concentration increases.

ZnO like many wide band gap semiconductors is thought to be self compensating. [2] Thus, it is difficult or impossible to consistently create p-type ZnO. If acceptors are introduced into ZnO, donor defects, most likely oxygen vacancies, spontaneously form in order to minimize the system energy.

The band gap of single crystal ZnO is measured to be between 3.2 and 3.3 eV. [24] Srikant *et al.*, however, assert that the true optical band gap is 3.3 eV and a valence band-donor transition often dominates at $\sim 3.15\ eV$. [92] The work function of ZnO:Al is reported to be $\sim 4.5\ eV$ by Minami *et al.*. [29] Swank measure the electron affinity of ZnO to be 4.57 eV by photoelectric measurement. [93]

Mobility is an important figure-of-merit. Generally, the larger the bulk mobility, the larger the channel mobility. The bulk mobility typically represents an upper limit for the channel mobility of an FET. Bulk mobility for single crystal ZnO at low doping densities is measured to be 150-200 cm^2/Vs. [68, 94] Typically, channel mobilities are much less than bulk mobilities, due to increased interfacial scattering rates and ZnO used in most TTFT processes is polycrystalline. The highest reported ZnO TTFT channel mobility is currently 7 cm^2/Vs. [3]

2.7.2 Energy Band Diagrams

Thin-film transistors (TFTs) generally behave in a similar way to bulk semiconductor transistors, with a few important exceptions. One way of distinguishing a TFT from a bulk semiconductor transistor is that TFTs are deposited onto an insulating substrate, whereas a bulk semiconductor transistor is constructed into a substrate via diffusion and/or ion implantion. However, perhaps a better and

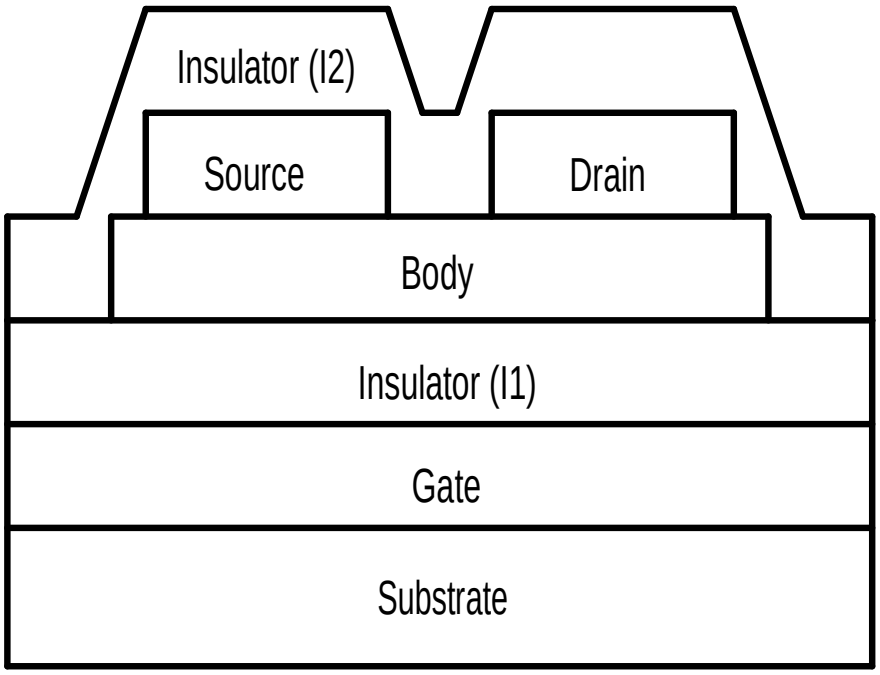

Figure 2.5: Schematic of a staggered bottom-gate with the source drain on top TTFT with the gate insulator labelled I1 and the backside insulator I2.

more device physics-oriented approach is to define a TFT as a transistor in which the back-side surface, *i.e.* the side opposite the gate, of the body can no longer be neglected when considering operation of the device.

A useful way to understand TFT operation is to consider how the back side interface may relate to transistor operation. For this purpose, consider Fig. 2.5 with insulators labelled I1 and I2. I1 is the gate insulator and I2 is the first-level interlayer dielectric, which in many cases is air. The interface between I2 and the channel forms the back side interface. Insulators I1 and I2 may tend to deplete or accumulate the body at zero bias, depending on the insulator chemical properties, interface properties, space charge, and gate metal to body work function difference. Thus, there are essentially four general cases, accumulation or depletion at the I1 body interface and accumulation or depletion near the I2 interface.

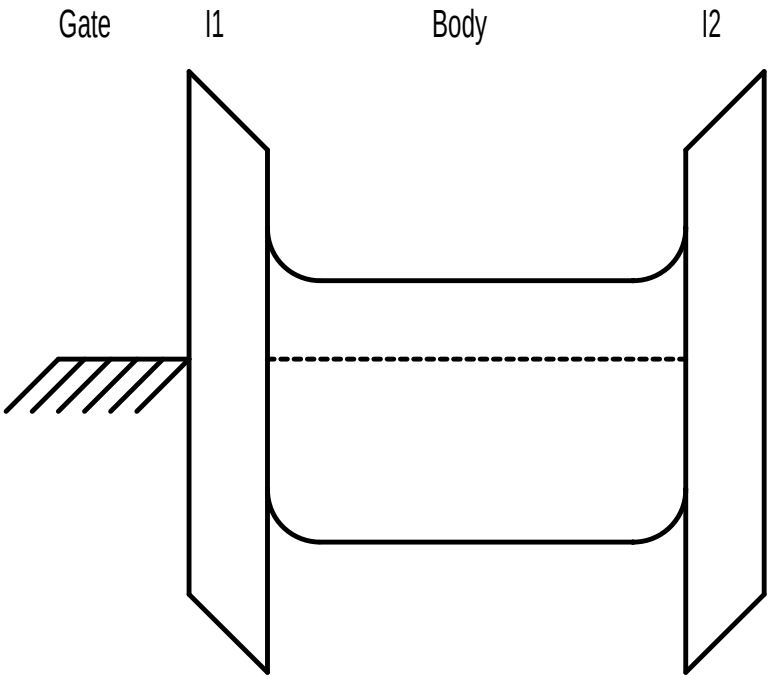

Figure 2.6: An energy band diagram of the body region of a TFT showing I1 and I2 depleting the body. In this example the depletion regions do not extend through the body, but only deplete the interfaces preventing a channel from forming.

First consider the case where both I1 and I2 deplete the body at zero bias, as shown in Fig 2.6. If the body doping density is large enough or the body is thick enough that the depletion regions do not extend through the entire body, a center channel may result, yielding a large off state leakage current. [95] For the case of lightly doped body materials the body is completely depleted , and the source to drain leakage is very low at zero gate bias. If I1 accumulates the body, resulting in a channel at zero gate bias, and I2 depletes the body a depletion-mode device results, as indicated in Fig. 2.7. Leakage in the off-state is small for this situation since the body/insulator interfaces are completely depleted, but a negative bias at the gate is necessary to deplete the channel.

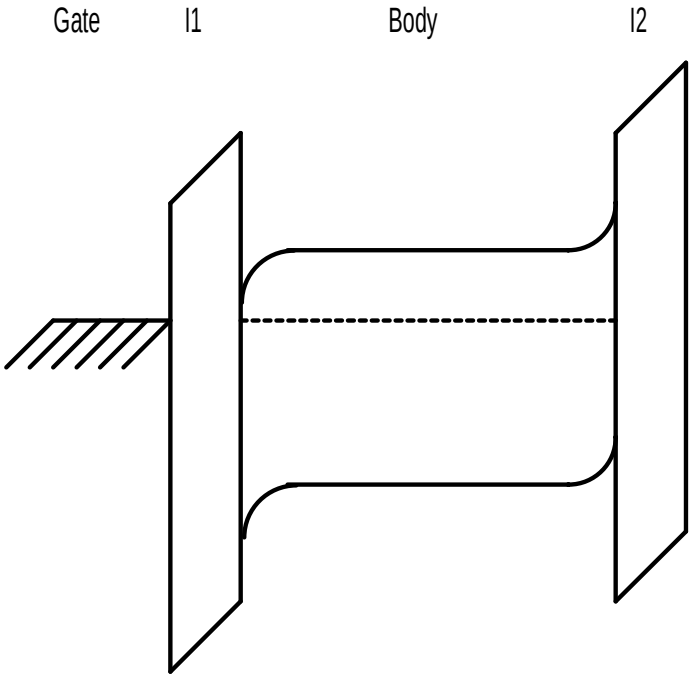

Figure 2.7: An energy band diagram of the body region of a TFT showing I1 accumulating the I1/body interface and I2 depleting the I2/body interface.

The situation in which I1 and I2, both accumulate the insulator/body interfaces, as shown in Fig. 2.8, is typically not very useful as a TFT since the back-side channel cannot be controlled by the gate electrode. I2 accumulation results in a large amount of leakage even at large off bias on the gate electrode. The result is similar when I1 depletes and I2 accumulates since the I2 channel cannot be turned off, as shown in Fig. 2.9.

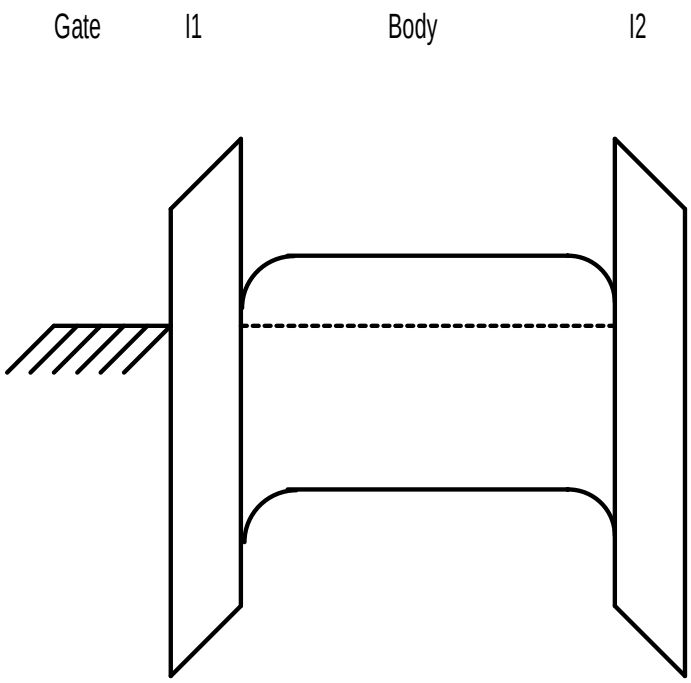

Figure 2.8: An energy band diagram of the body region of a TFT showing I1 and I2 accumulating the body, resulting in a channel at the I1/body and I2/body interface.

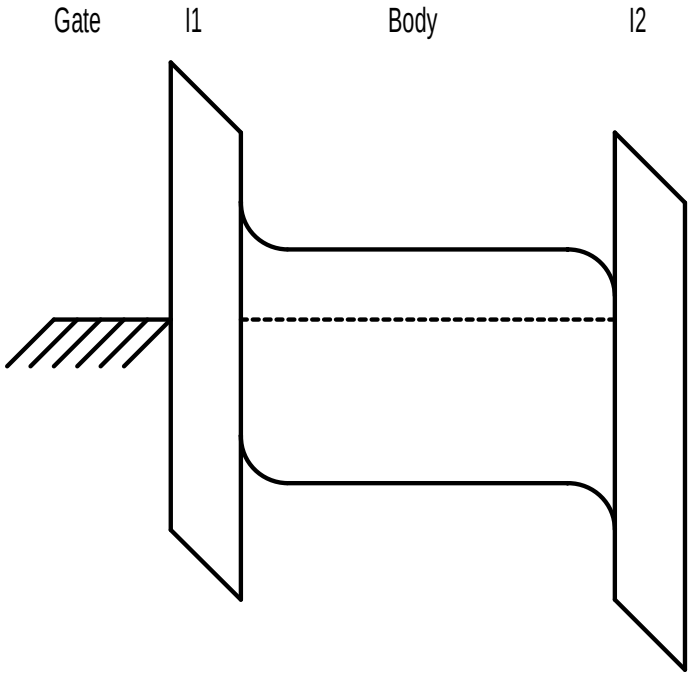

Figure 2.9: An energy band diagram of the body region of a TFT showing I1 depleting and I2 accumulating the body, resulting in a channel at the I2/body interface.

3. LIQUID PHASE DEPOSITION METHODS AND ZINC OXIDE TTFT INTEGRATION

3.1 Spin Deposition Methods

In principle spin-coating is a very simple deposition method. Processing methodology, spin speed, and acceleration control are parameters that must be controlled to deposited thin-films of consistent quality. Additionally, spin-coating deposition is particularly sensitive to ambient particles since the resulting thin-film is often tacky, and thus readily picks up particles.

A typical spin-coating process used in this dissertation is as follows:

1. Prepare the substrate for spin-coating. Typically ultrasonic cleaning for 40 min in 5 % Contrad^{TM} 70 in deionized water at 45°C.

2. Spin-coat solution. A typical program is 4000 rpm for 15 sec followed by 500 rpm for 60 sec.

3. Solvent bake. Typically 140°C for 30 min.

4. Conversion anneal. Parameters depend on solution used and desired final product.

Each step is tailored specifically to the substrate and thin-film to be coated. For example, some substrates such as silicon wafers with a layer of SiO_2 do not need a cleaning cycle.

3.1.1 Substrate Preparation

Without proper substrate preparation, poor films quality result. It is difficult to discern the whether poor film quality is due to substrate preparation, the spin solution, or the spin program. Often poor film quality is due to a combination of these three possibilities. A properly prepared substrate should be free of oils or particles, *i.e.* clean, and it should wet the solvent used in the spin solution (typically water). Since clean glass is hydrophilic, a good test of cleanliness of a glass substrate is to spray it with deionized water. If the water beads up and rolls off, *i.e.* if the surface is hydrophobic, the glass is dirty. If the water wets the glass, *i.e.* if the surface is hydrophilic, the glass is clean. However, not all clean surfaces are hydrophilic, *e.g.* many plastics are inherently hydrophobic.

A hydrophilic substrate is important for spin-coating many of the water based spin solutions used in research presented in this dissertation. Often water based spin solutions spin-coated onto a hydrophobic substrate will bead up and role off during deposition so that a thin-film is not deposited.

3.1.1.1 Ultrasonic Cleaning

Ultrasonic cleaning is an excellent and well-established method for cleaning substrates. It is aggressive enough to remove most types of dirty films and yet gentle enough not to damage the substrate. A typical cleaning solution is 5% Contrad^{TM} 70, a concentrated ultrasonic cleaning solution, and 95% deionized water. This ultrasonic cleaning solution is mildly basic, *i.e.* PH $\sim$ 8. Typically the solution is heated to $\sim 40^{\circ}C$ and then substrates are ultrasonically agitated for 40 min. After removing a substrate from the ultrasonic cleaner, it is thoroughly rinsed in deionized water and dried with nitrogen since cleaning solution that dries onto a substrate is

difficult to remove. Additionally, the concentrated surface layer of cleaning solution that remains as the water in the cleaning solution evaporates can damage the thin-film and the substrate.

Ultrasonic cleaning is the preferred method for substrate preparation, but is not always appropriate. If a substrate is inherently hydrophobic, ultrasonic cleaning does not always result in a hydrophilic substrate. Also, some thin-films are damaged by ultrasonic cleaning. For example, ATO is eventually completely removed if it remains in a Contrad^{TM} 70 cleaning solution for too long. Thus, any new material should be tested for compatibility with the ultrasonic cleaning action and solution before relying on it as a cleaning method.

Ultrasonic cleaning in Contrad^{TM} 70 is typically very effective at producing hydrophilic surfaces. Other cleaning methods explored for ATO-coated substrates do not produce a hydrophilic surface. However, after an ultrasonic clean in Contrad^{TM} 70 ATO films become hydrophilic. Thus, surfaces that are inherently hydrophobic will often become hydrophilic after ultrasonic cleaning. A possible explanation for this is that the ultrasonic cleaning solution leaves behind a hydrophilic hydroxide monolayer on the substrate surface. Thus, cleaning should be performed just before the film deposition step in order to minimize the opportunity for the surface to become re-contaminated.

3.1.1.2 Rapid Thermal Annealing and Ashing

Rapid thermal annealing (RTA) in oxygen is a cleaning procedure useful for removing organic contamination. In principle, organic contamination burns off with the application of heat and oxygen. This method, however, does nothing to remove inorganic films that do not break down at relatively low temperature ($< 700°C$).

Also, it is a relatively time consuming method since only four 1"x1" substrates can be cleaned in the RTA at one time. Additionally, this method is not a reliable method for producing hydrophilic substrates. Since this method has more drawbacks than advantages, it is generally avoided.

A related cleaning method is to expose a substrate to an oxygen plasma, *i.e.* ashing. Activated oxygen quickly removes any exposed organic material. Ashing is a very effective and often used method for removing photoresist (an organic polymer). Drawbacks to ashing, however, are similar to those for an oxygen RTA treatment; since ashing is not effective for inorganic contaminant removal or for producing hydrophilic surfaces.

3.1.1.3 Acetone, Methanol, and Deionized Water (AMD) Clean

Acetone, methanol, and deionized water (AMD) rinses, in that order, constitutes a commonly used and quick method for cleaning substrates and other thin-film equipment. It is a good method for removing a superficial build up of dirt and grease. Since there is no scrubbing action, as in ultrasonic cleaning, robust deposits are not removed. It is a good method for re-cleaning substrates that have been previously thoroughly cleaned, but have been handled since. For example, AMD cleaning is often used between thin-film deposition and a photolithography step. The major drawback to this cleaning method is that it can produce a large quantity of hazardous methanol and acetone waste.

3.1.1.4 Adhesion Layers

An adhesion layer may be useful when spin-coating onto hydrophobic films that cannot be cleaned or made hydrophilic in any other way. In addition, an

adhesion layer is also useful when an adhesion problem exits between the substrate or underlying film and the thin-film to be deposited. For example, HfO_2 does not adhere well to ITO but a thin layer ($\sim 10\ nm$) of PECVD SiO_2 prevents HfO_2 from delaminating.

Often PECVD SiO_2 is an excellent choice for an adhesion layer to an insulator layer, see Appendix B for a discussion of PECVD of SiO_2. Additionally, since SiO_2 is a hydrophilic material and is insulating, it can be used to prepare a hydrophobic substrate for spin-coating. When using SiO_2 as an adhesion layer in conjunction with another insulating film, the SiO_2 adhesion layer should be made as thin as possible, since the relative dielectric constant of SiO_2 is small at 3.8.

3.1.2 Spin-Coating

The spin-coaters used for the work presented in this dissertation are Berwer Science CEE models 100 and 100CB. The model 100CB is exactly the same as the model 100, except for the addition of a hotplate. They are fully programable and capable of storing a 10 step program. For each step the acceleration, spin rate, and time is precisely and repeatedly controlled. Thus, variation in the spin program is almost nonexistent.

A typical spin program consists of a dispense step, a high speed spin, and a low speed drying spin. Dispensing with the substrate spinning at a low rpm (< 500 rpm) produces very poor film coverage. A better method, the method used in this work, is to dispense enough solution to cover the majority of the substrate with the substrate stationary, and then to ramp up to the high speed spin. Dispensing with the substrate spinning could work well if a dispenser fixture was available on the spin-coater used for the work presented in this dissertation.

During the high speed spin the substrate is quickly spun up to a high speed (typically 2000–3000 rpm). Generally, the faster the spin speed, the better the film uniformity, within a practical limit (typically 4000–5000 rpm). Also, the faster the speed of the high speed spin, the thinner the film. Typically, for speeds less than ~ 2000 rpm, the spin is not fast enough to adequately spread out the solution and evaporate the solvent, resulting in poor film uniformity. Additionally, the acceleration to the high speed spin helps to spread the spin solution. Generally, the larger the acceleration rate, the better the solution is distributed, but a large accelerations also significantly increases motor and bearing wear.

Finally, the drying step drives out most of the remaining solvent in the thin-film. The drying step typically consists of a 500 rmp spin for 1 min. This step is generally not used for photoresist deposition, but is very advantageous for the deposition of films which employ low volatility solvents. Many of the solutions explored in this dissertation use water as the primary solvent and water is a low volatility solvent compared to most photoresist solvents. Thus, the drying step is often used for water-based spin solutions.

3.1.2.1 Incomplete Coverage

Perhaps the most common problem associated with spin-coating is incomplete coverage. Typically, the film takes the appearance of a splatter mark where some areas are covered with a film and others are not. Incomplete coverage may result if the substrate is accelerated too slowly or the final spin speed is too slow to adequately spread the spin solution. Generally, a spin speed of at least 2000 rpm is required to completely spread most spin solutions. Incomplete coverage may also

result if there is poor adhesion between the solution and substrate due, for example, to having a dirty substrate, an incompatible substrate and solution.

3.1.2.2 Particle Defects

Cometing is usually observed after spinning a particle-contaminated spin solution. [96, 97] Streaks appear with a particle at the head of the comet and a tail pointing radially outward. Pinholes are sometimes observed instead of or along with comets. Typically, a particle sits in the center of a circular void or pinhole. Particles may also result in a rough spin-coated film if the solution easily flows over and around the particles. Particle-related issues may avoided be filtering the spin solution just prior to spin-coating. Typically, a 0.4 μm filter attached to a syringe works well to filter the spin solution.

3.1.2.3 Chuck Marks

Chuck marks appear as a result of heat transfer between the spin chuck and the substrate. [96, 97] Variation in thermal contact between the chuck and the wafer results a concomitant variation in the evaporation rate of the spin solution. Thus, the chuck pattern is transferred to the thin-film as a slight thickness variation. Chuck marks can be eliminated or reduced by changing the chuck and/or the substrate. Generally the appearance of chuck marks indicates only a small variation in film thickness. Thus, chuck marks are not usually a concern unless film thickness uniformity is critical.

3.1.2.4 Crystallization

Crystallization is a problem that may be encountered as a new spin solution is developed. As the solvent in the spin solution evaporates, either during the spin or the solvent bake, the thin-film may begin to crystallize. Crystallization often results in a textured pattern, causing the film to appear hazy. Observations with an optical microscope often reveal snowflake or geometric patterns, *e.g.* hexagons, indicating crystallization. Crystallization may be prevented by adding a stabilizer or changing the source material of the spin solution.

3.1.3 Spin Solution Bake

During the empirical phase of investigation it was observed that the temperature ramp rate was a primary variable in establishing the visual clarity of the thin-film, *i.e.* hazy or clear appearance. For example a 1"×1" substrate with a zinc nitrate based thin-film placed in a room temperature oven would often become hazy as the temperature increased, where a 2"×2" substrate would not. In addition, hazy patterns would often appear in the shape of the ceramic piece they were placed on. These effects were attributed to thermal gradients caused by the size of the substrate and the shape of the piece they were placed on. To avoid issues related to thermal gradients all ovens and hot plates were heated to temperature before the substrates were introduced. In addition, large ceramic disks were placed in the oven upon which the substrates were placed, in order to prevent a heat gradient across the substrate.

3.1.3.1 Solvent Bake

Typically spun-on films are gently dried in an air oven or hot plate for 1–30 *min* immediately after the spin-coating. [98] The purpose of this bake is to drive out any remaining solvent and to harden the film. This bake should be done at a low enough temperature so that oxide conversion does not take place. A typical drying temperature for most of the work presented in this dissertation is $140°C$.

3.1.3.2 Conversion Bake

The conversion bake is used to convert the spun-on precursor solution to its desired material state, *e.g.* zinc nitrate to ZnO. A conversion bake may consist of a single thermal cycle in one process gas or multiple thermal cycles in different process gasses. For example, conversion to an oxide may be accomplished with a single bake in air or oxygen, but conversion to a sulfide may require conversion to an oxide then a bake in a sulfurizing gas.

The conversion bake is a critical step in determining the final material properties of the thin-film, including crystallinity and stoichiometry. The optimal conversion bake depends on the desired film material and spin solution used. For the zinc nitrate-based solutions explored in this dissertation, both RTA and air furnace annealing are used for conversion. The advantage of the RTA is that the gas flow rate, temperature ramp, and temperature are precisely controlled. With the air furnace, there is more variation in the process gas and temperature, but the bake time may be much longer than with the RTA. A detailed discussion of the results of various conversion bakes is given in Chapter 4.

3.1.4 Solution Preparation

Solution preparation is one of the most difficult steps of spin-coating development since many variables exist for a given solution. The solvent must wet and stick to the substrate as discussed Sec. 3.1.1. Also, the solvent cannot evaporate too quickly or too slowly. Fast evaporation leads to inconsistency in the spin solution since it is not possible to dispense the spin solution and start the spin before a significant portion of the solvent has evaporated. Slow evaporation leads to incomplete drying while spinning and as a result the resin may still be semi-liquid after the spin is complete. Additionally, it is desirable to have a spin solution that is nontoxic so that a minimum amount of protective gear is required and waste may be disposed of without harm to the environment.

The spin solution needs to be as clean, dirt free, and homogeneous as possible. Particulates in the resin produce comets or pinholes. Also, an inhomogeneous spin solution results in inconsistencies from one spin to the next; this is usually is avoided by shaking the solution before each deposition. Air bubbles in the solution can behave in a very similar manner to particles and should be avoided whenever possible.

Solution viscosity must also be carefully controlled since the final film thickness is dependent on the viscosity. The more viscous the solution, the thicker the spun-on film. The relation between final thickness and viscosity is usually best found empirically for a new spin solution since many factors contribute to the final thickness and it is not always possible or efficient to accurately predict the thickness from the solution viscosity. Process models for spin-coating, however, have been developed. [22, 23]

The solvent bake and conversion annealing conditions are also important parameters of the spin solution recipe. The thin-film must not crack or become rough in either the solvent bake or the conversion bake. Cracks and roughness can be caused by crystallization, film stress, thermal gradients, or thermal shock. Thus, sometimes cracking and roughness can be eliminated by changing the way the conversion bake and solvent bake are performed.

A spin solution typically consists of three types of constituents: source material, solvent, and stabilizer/thickener. The source material is the precursor for the thin-film desired. Example source materials for ZnO are zinc acetate or zinc nitrate. Additionally, the source may consist of a dopant material such as $CuCl_2$. The source material is chosen so that it converts cleanly and at a reasonable temperature for the substrate and application desired.

The solvent should wet the substrate. Since water is the solvent for many of the spin solutions used in this dissertation, the substrate should be hydrophilic. The source material must also have a high solubility in the solvent and ideally viscosity should vary strongly with source material concentration. The solvent should also be chosen so that the vapor pressure is appropriate for spin-coating. A high vapor pressure may result in significant evaporation before the spin has stabilized, resulting in a nonuniform thin-film. A low vapor pressure solvent results in a wet or tacky thin-film. Sometimes two solvents may be used together in order to get the best characteristics of both. For example, a water-methanol mix my be used to increase the vapor pressure, increase the wettability to the substrate, and modify the solubility.

A stabilizer/thickener is not always necessary, but for some spin solutions it is not possible to obtain all of the desired properties from just a source material and a solvent. Often a stabilizer/thickener is added to a solvent to improve the

solubility of the source material. For example, soap improves the solubility of grease in water. Thus, soap acts as a stabilizer for the grease. Additionally, it is often not possible to get the viscosity necessary for spin-coating by adding more source material to a solvent. In this case a thickener may be used to increase the viscosity; often this is accomplished by forming a polymer with the source material. Finally, a stabilizer/thickener may be used to inhibit crystallization, as discussed in Sec. 3.1.2.4.

3.1.4.1 Zinc Nitrate-Based Spin Solution

The ZnO spin-coating method developed in this dissertation is based on a spin solution of water, glycine, and zinc nitrate. A key advantage of this spin solution over those proposed by other groups is that it is capable of producing films of 100-150 nm in a single spin deposition. [47, 48, 49, 50, 51, 52, 53, 54, 55, 56, 57, 58, 59, 60, 61, 62, 63, 64, 65] Spin solutions investigated by other research groups, based on zinc acetate, require multiple spins in order to produce 100 nm thin-film. Typically, zinc acetate-based spin solutions can only produce $\sim$ 10 nm films per deposition. Clearly, a spin solution that can produce a useful film thickness in a single deposition is desirable for processing, integration, and manufacturablity.

Spin solutions attempted with water and zinc nitrate only tend to crystallize as the water evaporates. This produces extremely rough films that not electrically or optically useful. Thus, glycine is added to improve the spin properties and inhibit zinc nitrate crystallization. Glycine increases the viscosity of the spin solution, thus thicker spin solutions are possible. Glycine, however, is not desirable in the final ZnO film and must be burned off while the zinc nitrate is converted to ZnO. This is accomplished either with a prebake of $260°C$ or during the final conversion bake.

During the prebake, the glycine acts as a reductant and nitrate as an oxidant to burn the drying spin solution, leading to conversion to ZnO. Incomplete glycine burn will result in carbon contamination in the ZnO film. The spun on zinc nitrate films are fully converted to ZnO by a final high temperature bake or RTA (400-700°C). The effects of the prebake and final bake on ZnO film quality are discussed in Sec. 4.2.1.3

Occasionally, ZnO films take on a cloudy appearance during the final bake. This occurs when the films are placed in a cold oven and allowed to slowly heat up, or there is a heat gradient at the substrate as it heats up. A cloudy appearance may be due to zinc nitrate crystallization as the glycine burns off, or cracking, or both, resulting in film roughness. Film cloudiness is easily prevented by placing the films in a hot oven or using an RTA. The film should be move directly from the spin-coater to a preheated hot plate to, a preheated furnace, or an RTA. Ideally, spun-on films should not be allowed to cool between heating steps.

The zinc nitrate precursor solution for this dissertation is prepared in the following method, unless otherwise noted. First, 3.6 parts by mass of 99.999% zinc nitrate hexahydrate from GFS Chemicals are mixed with 1 part of 99.7% glycine from Alfa Aesar and 2.2 parts of 18.2 $M\Omega/cm$ deionized water. The solution is then placed in a boiling water bath for 75 min. The solution decreases in volume by $\sim 10\%$ during the heating cycle. The spin solution is subsequently diluted with deionized water to a percentage of the original solution to deionized water.

3.1.4.2 Zinc Acetate Based Spin Solution

Zinc acetate is the precursor of choice for most sol-gel research. The zinc acetate-based solution used in this dissertation consists of zinc acetate source mate-

rial and methanol as the solvent. [62] Zinc acetate-based solutions typically result in the deposition of very thin layers, so that multiple coatings are often required to build up layers of appropriate thickness ($\gtrsim 20\ nm$). In this dissertation, 0.055–0.3 M solutions of zinc acetate in methanol are investigated and the results are discussed in Sec. 4.2.3.

Typically zinc acetate based spin solutions are spun or dip-coated. Then, a low temperature ($\sim 100°C$) bake is performed, followed by a high temperature ($\sim 600°C$) conversion bake. Omitting the solvent bake is found to result in yellow films, presumably due to carbon contamination from methanol combustion in the film.

3.1.4.3 Hafnium-Based Spin Solutions

Three concentrations of Hafnium-based spin solutions are explored. Solution A and B are prepared by mixing 6.14 g of $HfOCl_2 \bullet 8H_2O$ with 1.24 g of glycine and 3.3 mL of deionized water. The solution is then boiled for 1.25 hrs. Finally, 0.58 mL of deionized water is added to solution B. Solution A is not diluted with deionized water. Solution C is prepared by mixing 4.96 g of $HfOCl_2 \bullet 8H_2O$ with 1 g of glycine and 3.6 mL of deionized water. The solution is then boiled for 1.25 hrs. Finally, 2.95 mL of deionized water is added to solution C.

3.1.4.4 Strontium Nitrate-Based Spin Solutions

Strontium Nitrate films spin-coated on to SrS as discussed in Sec. 4.1. The best SrS thin-films are obtained by mixing 9 g of $Sr(NO_3)_2$ with 30 mL of ethanol and 36 mL of deionized water.

3.1.4.5 Magnesium Nitrate-Based Spin Solutions

Magnesium nitrate-based spin solutions are very similar to zinc-nitrate based spin solutions. Thus, optimal magnesium nitrate-based spin solutions are obtained by using the recipe discussed in Sec. 3.1.4.1 for zinc nitrate-based spin solutions, but replacing zinc nitrate by the same mole ratio of magnesium nitrate. Scaling the amount of magnesium nitrate by the ratio of the molar weight of magnesium nitrate to zinc nitrate, *i.e.* add 0.86 as much magnesium nitrate by mass as you would zinc nitrate.

3.1.4.6 Organic Spin Solutions

Organic based spin solutions cover a broad class of materials used in the integrated circuit and other industries. Typically they consist of a polymer in a solvent. Solution viscosity is controlled by the polymer concentration and the amount of polymerization. Often only a solvent bake ($\sim 100°C$) is required to remove the solvent, *e.g.* photoresist and polyamide, but some organic materials require a conversion bake as well, *e.g.* PPV for PLEDs, as discussed in Appendix A.

3.2 TTFT Processing

3.2.1 TTFT Geometry

TTFT geometry plays an important role in establishing both the device performance and the process flow for device fabrication. Generally, the following criteria should be considered when selecting a TTFT geometry: process compatibility, gate insulator planarity, minimizing the source and drain parasitic resistance, and mini-

mizing parasitic capacitances. Process compatibility means that each thin-film layer must be compatible with the previous and following layer, chemically, mechanically, and thermally. Thus, each layer should not chemically react significantly with adjacent layers. Additionally, each layer should bond strongly enough with the previous and the following layer to overcome mechanical film stress and prevent delamination. Finally, a layer requiring a high temperature anneal should not be deposited on top of a layer that can only tolerate a low temperature anneal.

Gate insulator planarity is important in minimizing high electric field areas that may promote insulator breakdown. It is critical for TTFT operation that the gate insulator tolerate as large an electric field as possible so that a channel may be induced without breaking down the gate insulator. Additionally, TTFT planarity generally improves the uniformity of the gate insulator and body layer.

A large source and drain resistance results in drain current limiting, which should be avoided. Larger contact areas between the source and drain contacts and the body result in smaller current densities thus lowering source and drain resistance.

Parasitic capacitance slows down the response time of a TTFT structure. [2] It may be reduced by minimizing the overlap between the source and drain regions and the gate, and by reducing TTFT dimensions.

3.2.1.1 Bottom Gate

In a bottom-gate TFT structure, the gate is deposited first and therefore a high-quality gate insulator is more easily produced. Planarity and surface roughness issues related to the material under the gate are minimized since there is only the substrate underneath the gate. Additionally, the gate insulator may be chemically prepared and cleaned prior to spin-coating the body.

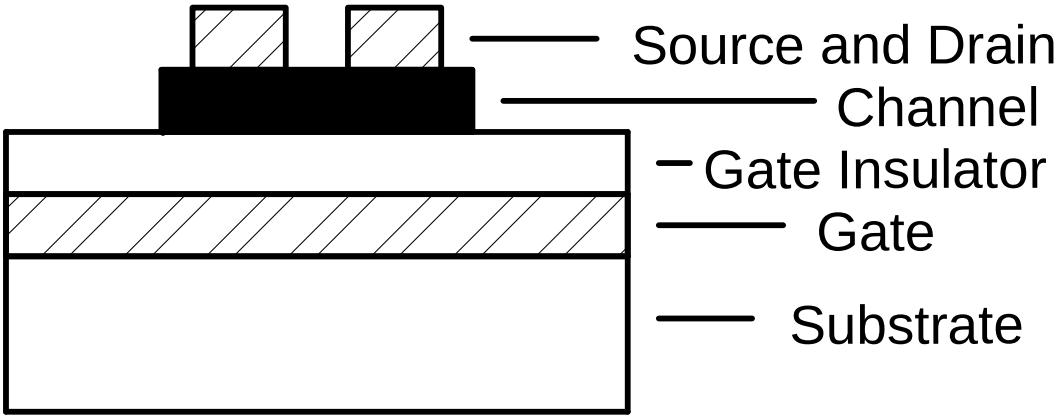

Figure 3.1: A schematic of a bottom-gate, source and drain on top TFT structure.

With the source and drain on top, as shown in Fig. 3.1, the parasitic source and drain to gate capacitances are reduced since the distance between the source and drain contacts and the gate is maximized. However, the source and drain resistance due to the body will be large since current must pass through the body to reach the channel. A processing draw back of this configuration is that the source and drain must be patterned with lift-off since a wet etch will have a faster etch rate for the ZnO body than the ITO source and drain.

Placing the source and drain on the bottom, as shown in Fig. 3.2, allows patterning of the ITO source and drain with a wet etch. The source and drain to gate capacitance, however, is increased since the source and drain are now closer to the gate. Additionally, the source and drain resistance is in part increased since the effective contact area to the channel is limited to the edges of the source and drain. However, the source and drain resistance due the bulk conductivity through the channel is minimized. The overall planarity of this structure is very good since fewer patterned layers are stacked on each other; this may be an important advantage as interconnect layers are added. Spin-coating of the body layer is more difficult when

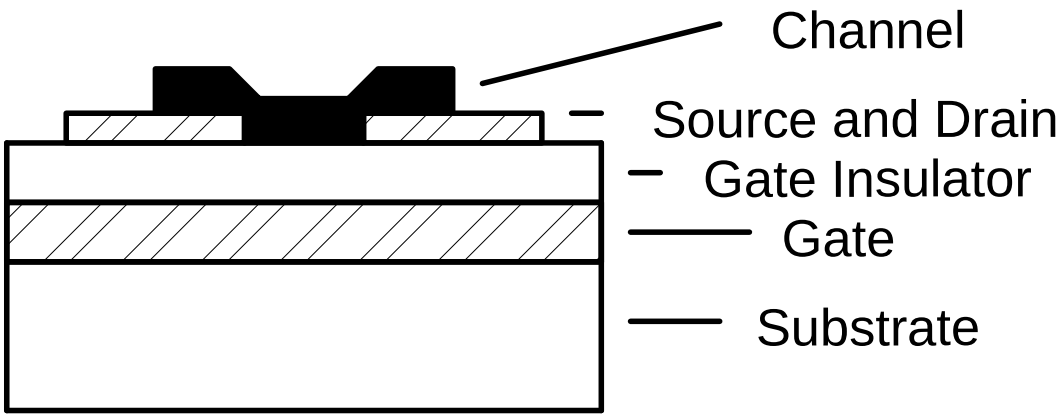

Figure 3.2: A schematic of a bottom-gate, source and drain on bottom TFT structure.

this structure is used since the surface being coated is not planar. This may result in spin solution adhesion problem and cometing near the source, drain, and the gate insulator.

3.2.1.2 Top Gate

A top-gate TFT structure offers few advantages over a bottom gate structure since the gate must be deposited over an often rough and non-planar body surface. Additionally, the interaction between the substrate and the body may result in a backside accumulation layer, as discussed in Sec. 2.7.2.

Similar to the bottom-gate with source and drain on bottom structure, the top-gate with source and drain on bottom structure, shown in Fig. 3.3, allows for the use of a wet etch to form the source and drain, since the source and drain are below the ZnO body. Source and drain to gate capacitances are small for this structure since they are positioned further away from the gate. Source and drain

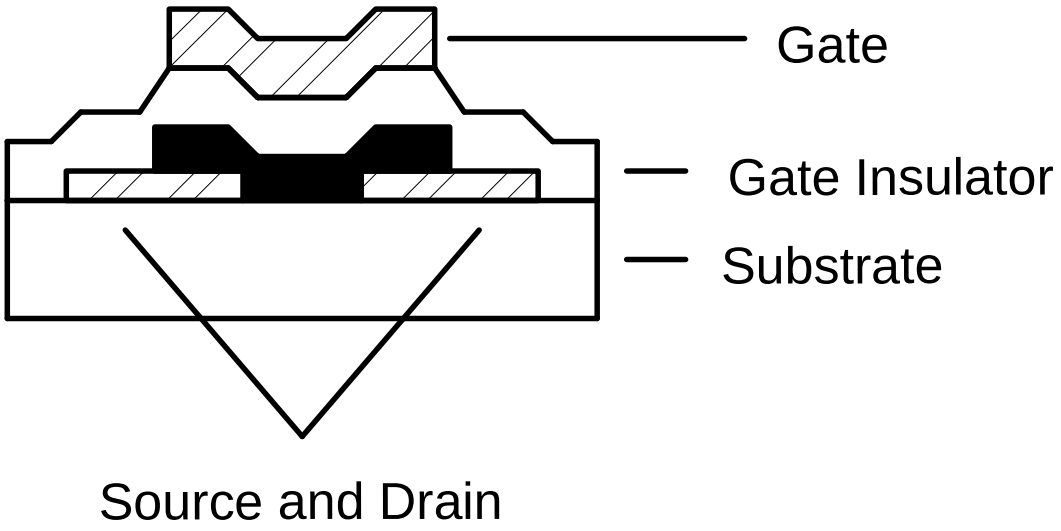

Figure 3.3: A schematic of a top-gate source and drain on bottom TFT structure.

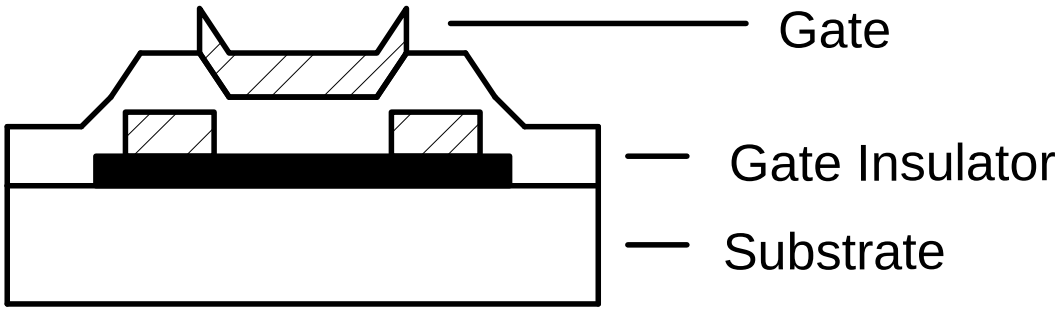

Figure 3.4: A schematic of a top-gate source and drain on top TFT structure.

resistances should be similar to that of a bottom-gate with source and drain on top structure of the same geometry

Lift-off must be used to pattern the source and drain of the top-gate, source and drain on top structure shown in Fig. 3.4. The source and drain contact to the body region should be very good with this structure, but the source and drain to gate capacitance is also large.

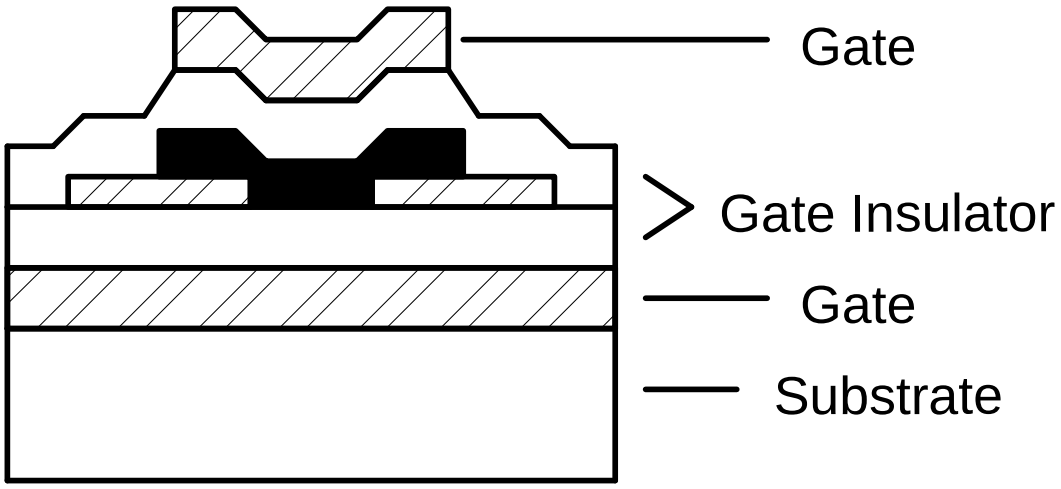

Figure 3.5: A schematic of a double-gate TFT structure.

3.2.1.3 Double-Gate

The double-gate structure, as shown in Fig. 3.5, has all of the processing disadvantages of top and bottom gate structures and it is more complex. However, a double-gate structure offers several advantages. The drain current on-to-off ratio is improved, since a channel is induced on both sides of the body layer in the on state. Additionally, the drive current is essentially doubled at a given voltage compared to a single-gate TFT structure of identical dimensions. Finally, the double-gate structure provides control over the backside channel region so that an insulator body interface that normally accumulates the body when floating can now be biased so that the channel is depleted. Thus, the passivation problem, *i.e.* creating a non-accumulating backside insulator body interface, is much simpler to solve with the double-gate structure.

3.2.2 TTFT Substrates

Proper substrate selection and preparation is important to the functionality of any subsequently-deposited layers of a TTFT structure. First, it is essential that the substrate be clean and free of any contamination, as discussed in Sec. 3.1.1. The crystal orientation of the substrate also plays an important role in establishing the crystal orientation of subsequent layers. [41] Additionally, transparency of the substrate establishes an upper transparency limit for any TTFT structure. Thus, it is important to select a substrate which is as transparent as possible. Also, the maximum annealing that a substrate can tolerate establishes the maximum annealing temperature for any subsequent layer. Finally, adhesion should be good and coefficients of thermal expansion should be similar, in order to prevent cracking and delamination.

In this dissertation four types of substrates are used for making various types of TTFTs and test structures: silicon wafers, Corning^{TM} 1737 glass, ITO coated Corning^{TM} 1737 glass, and ATO/ ITO-coated Nippon Electric Glass (NEG). [99] Silicon wafers are high quality, inexpensive, very clean, very flat, single crystalline, available with varying conductivity, and can withstand annealing temperatures up to $\sim 1415°C$. Additionally, it is possible to grow a high-quality thermal oxide on a silicon wafer. [68] Thus, a silicon wafer is a nearly ideal substrate. However, silicon wafers are not transparent, and thus cannot be used for TTFTs. Still, they are useful for assessing material properties and transistor electrical properties when transparency is not required. In this dissertation, silicon wafers are used only to assess troublesome spin solutions, as discussed in Sec. 4.3.

Corning^{TM} 1737 glass is an excellent electronic grade glass substrate. It is amorphous, relatively free of impurities, transparent, readily available, inexpensive,

and able to withstand anneals of up to $\sim 900°C$. Additionally, clean glass provides a hydrophilic surface for spin-coating. It may also be purchased with or without a thin-film of ITO.

ATO and ITO coated NEG is provided by Planar Systems, Inc. . ATO is an excellent insulator for TTFT work, as discussed in 2.5. The NEG is amorphous, relatively impurity free, transparent, and able to withstand anneals up to $700°C$ (anneals up $850°C$ are possible although with increasing delamination and warpage problems). The main drawback of this substrate is that it is not commercially available with an ATO coating and thus of limited long-term usefulness for TTFT development.

3.2.3 Transparent Conductor Processing

Transparent conductors make up the gate, source, drain, and will eventually be used as the interconnects of TTFT technology. In this dissertation, ITO is used as a transparent conductor since it is highly transparent, readily commercially available, highly conductive, and forms an efficient injecting contact to ZnO. [1, 2]

ITO may be deposited via ion-beam sputtering, RF sputtering, and spin-coating. [79, 89, 100] Typically, in the work presented in this dissertation ITO-coated glass is employed, either as Corning^{TM} 1737 glass with an ITO layer or as NEG with a layer of ITO and ATO. [99] Additionally, thin-film layers are deposited via ion-beam sputtering, unless otherwise noted. Ion-beam sputtering offers high throughput and provides consistently high quality ITO. The ITO in this dissertation is ion-beam sputtered from a 6" ITO target with a beam current of 0.6 A in an 80% Ar and 20% O_2 atmosphere. Typical deposition rates are $\sim 10\ nm/min$. Ion-beam

sputtered ITO is typically RTAed in oxygen at $300°C$ to improve the transparency of as-deposited ITO.

ITO may be patterned, with some difficulty, using lift-off or very nicely using an HCl wet etch. ITO does not tend to break off cleanly with lift-off; often hangers and spires are left over for critical dimensions smaller than $\sim$ 50 μm. A short ultrasonic clean, however, in deionized water removes most of the hangers. [13] The lift-off process for ITO is as follows:

1. Photolithography with ITO layer mask. Note that ITO remains where photoresist does not cover the substrate.
2. ITO deposition. The ITO film should be much thinner than the photoresist film.
3. Acetone, methanol, deionized water (AMD) rinse. It is often necessary to soak the substrate in acetone to remove all of the photoresist. An optical microscope is useful in assessing when the photoresist has been completely removed.
4. Ultrasonic clean for 1 min in deionized water. This step should be as short and gentle as possible in order to prevent damage to underlying layers. This step is intended to simply break off any ITO hangers and spires.

When it is possible, wet etching of ITO is preferred to lift-off patterning. The wet etch rate of ITO is strongly dependent on ITO processing parameters. For example, S.A. Bashar reports an etch rate of $\sim$ 1 nm/sec with $\sim$ 18% HCl. [101] Etching ion-beam sputtered ITO deposited at Oregon State University, however, results in an etch rate of $\sim$ 0.1 nm/sec when $\sim$ 16% HCl is used. Thus, the ITO etch rate should be empirically verified for each deposition recipe and processing method.

Sometimes it is convenient to use Al as a source and drain contact during TTFT development, even though it is not transparent. Al forms an injecting con-

tact to ZnO. Additionally, Al is far simpler than ITO to process since Al can be deposited via thermal evaporation. Also, Al does not require a post-deposition anneal. Typically, Al is only used in TTFT development, so that it is patterned using a shadow mask.

3.2.4 Insulators and Passivation

Thus far, ATO is the insulator of choice for TTFT applications since it is compatible with ZnO, has a relatively large dielectric constant, and exhibits extremely low leakage. It is, however, not commercially available and cannot be deposited at Oregon State University. Also, a method of patterning ATO is not currently available. Thus, it is imperative for TTFT development to find a readily available insulator.

Preliminary investigation of SiO_2 via PECVD for TTFT applications, as discussed in Appendix B, is not promising. SiO_2 is a poor choice as a gate dielectric since it has a small relative dielectric constant of 3.8. Also, the work of Masuda *et al.* indicates that SiO_2 is not compatible with ZnO. [6]

Preliminary work on spin-coating HfO_2, as discussed in Secs. 4.3, indicates that it is well suited for TTFT applications. However, it is too soon to tell if HfO_2 will be a viable choice for TTFT gate insulator applications. The results of Nomura *et al.* indicate that HfO_2 greatly improves $InGaO_3(ZnO)_5$ TTFT performance. [4]

Passivation, *i.e.* coating the TTFT with an inert protective layer, is an issue closely related to that of the TTFT gate insulators, since a good gate insulator will likely function as a good passivation material. Passivation should protect the TTFT from damaging materials in the ambient environment and preserve TTFT operation. Thus far, all attempts to passivate ZnO TTFTs have produced backside

channels, thus degrading off-performance of the device, as discussed in Secs. 2.7.2 and 5.4.

3.2.5 Body

A goal of this dissertation is to spin-coat ZnO as a body material for TTFTs. How this is accomplished is discussed in Chapter 4. Ion-beam sputtered ZnO bodies are used as a baseline to compare to spin-coated ZnO. ZnO is ion-beam sputtered using a 6" undoped ZnO target with a beam current of 0.6 A in an 80% Ar and 20% O_2 atmosphere. Typical deposition rates are $\sim 10\ nm/min$.

ZnO is easily patterned by lift-off, without the need for an ultrasonic clean to remove hangers and spires. However, lift-off is not an option for spin-coated ZnO. ZnO is wet etched with HCl at a rapid rate. It is likely that other etch solutions would produce a more controlled etch of ZnO, but since small critical dimensions are not required in the body layer a precise etch is not required. With a $\sim 2.4\%$ HCl solution, the ZnO etch rate is $300\ nm/min$.

3.2.6 Process Integration

During the development of a new process it is important to keep in mind how materials may be processed together, as shown in Table 3.1. For each material used in the TTFT process, one needs to consider how it can be deposited, annealed, and patterned. The maximum annealing temperatures listed in Table 3.1 are based primarily on the melting temperature of a given material and should only be used as a guide. Many materials warp, sublimate, and otherwise decompose much below their melting temperature.

Table 3.1: Important process integration properties for various materials and substrates used in the TTFT process. †denotes a substrate.

Materials	Deposition method	anneal required	max. anneal	Etch	lift-off	References
ZnO	Ion-beam,	$\geq 600°C$, O_2	$\sim 2000°C$	HCl	good	[14, 102]
	RF sputter	$\geq 600°C$, O_2	$\sim 2000°C$	HCl	no	[14, 102]
	spin-coating	$\geq 600°C$, air	$\sim 2000°C$	HCl	no	[14, 102]
ITO	Ion-beam,	$300°C$, O_2	$\sim 1600°C$	HCl	poor	[14, 102]
	RF sputter	$300°C$, O_2	$\sim 1600°C$	HCl	no	[14, 102]
	spin-coating	$400°C$, air	$\sim 1600°C$	HCl	no	[14, 79, 89, 100, 102]
Al	evaporation	none	$\sim 600°C$	NaOH	poor	[14, 102]
	Ion-beam	none	$\sim 600°C$	NaOH	poor	[14, 102]
SiO_2	PECVD	none	$\sim 850°C$	HF,RIE	N/A	[14, 102]
Corning^{TM} 1737†	N/A	N/A	$\sim 900°C$	HF,RIE	N/A	[103, 104]
NEG/ITO/ATO†	N/A	N/A	$\sim 700°C$	HF,RIE	N/A	[99]
Si Wafer†	N/A	N/A	$\sim 1400°C$	wet, dry	N/A	[14, 68, 102]

Any time an anneal, etch, clean, *etc.* is considered in a process, its effect on all other layers in the device must be considered. A substrate clean may actually function as an etch for a given thin-film. For example, the Contrad^{TM} 70 clean used as an ultrasonic cleaner completely removes ATO over time. Additionally, the selectivity of each etch must always be considered. For example, HCl is an etchant for both ZnO and ITO but the etch rate of ZnO is much greater. Thus, HCl is a selective etchant for ZnO.

Generally the glass substrate used in the TTFT process determines the maximum annealing temperature, which is established by the glass melting temperature and softening point. However, the effects of thermal cycling on all layers should always be considered, since thermal cycling can promote impurity migration and chemical reactions well below the melting temperature of any given layer.

3.2.7 Photolithography

Unique challenges exist when attempting to do photolithography with transparent materials and substrates. Typically, visible light is used to visually align a mask to a perviously deposited layer. However, since all of the layers of a TTFT are transparent to visible light, it is extremely difficult to see the alignment marks of a transparent layer. Adjusting the focus and lighting often gives enough contrast for alignment, but layers thinner than $\sim 20\ nm$ are extremely difficult to align. A black and white camera attached to the mask aligner microscope can also aid in alignment since the contrast is often better than with the naked eye. It is essential that the mask aligner optics are clean, well maintained, and well adjusted since it is critical that the view of the mask and substrate are as clear as possible.

The transparent nature of the substrate and thin-films also results in UV light passing completely through the substrate, and perhaps being reflected back. This can result in ghost images and/or over-exposure of the photoresist. Thus, an opaque backing should be placed behind a transparent substrate to minimize back reflection. TTFTs fabricated for this dissertation are aligned using a Suss MJB3 equipped with black teflon coated chucks designed to minimize back reflection. Care should be taken to minimize scratches and particulates on the chuck surface as they can affect the back reflection.

In this dissertation, a photolithography process for a bottom-gate, source and drain on top structure is developed. The masks are provided courtesy of Dr. M. Subramanian and were originally designed for HFET work. [105] A positive and negative of each mask is available so that lift-off or etching can be used without the need to switch from a positive to a negative resist. The masks available provide structures with width (W) to length (L) ratios of 2/1 and 8/1, as shown in Fig. 3.6.

The following recipe is used for the photolithography process which employs the masks described above:

1. Spin Shipley S1813 photoresist onto a substrate at 4000 rpm for 30 $sec.$ [106]

2. Bake on the Model 100CB hot plate for 1 min at 115°C in contact mode, *i.e.* no vacuum or nitrogen cushion.

3. Align the HFET mask to the previous layer and expose for 10 sec. The lamp should be optimized for a peak output of 18.1 MW/cm^2 at 365 nm.

4. Develop the photoresist by submerging the substrate in a solution of 5 parts deionized water to 1 part Shipley Microposit®351 developer for 1 min. [107]

5. Rinse the substrate thoroughly with deionized water and dry it with nitrogen.

6. Perform etch or deposition, as necessary, and remove the photoresist with an AMD clean.

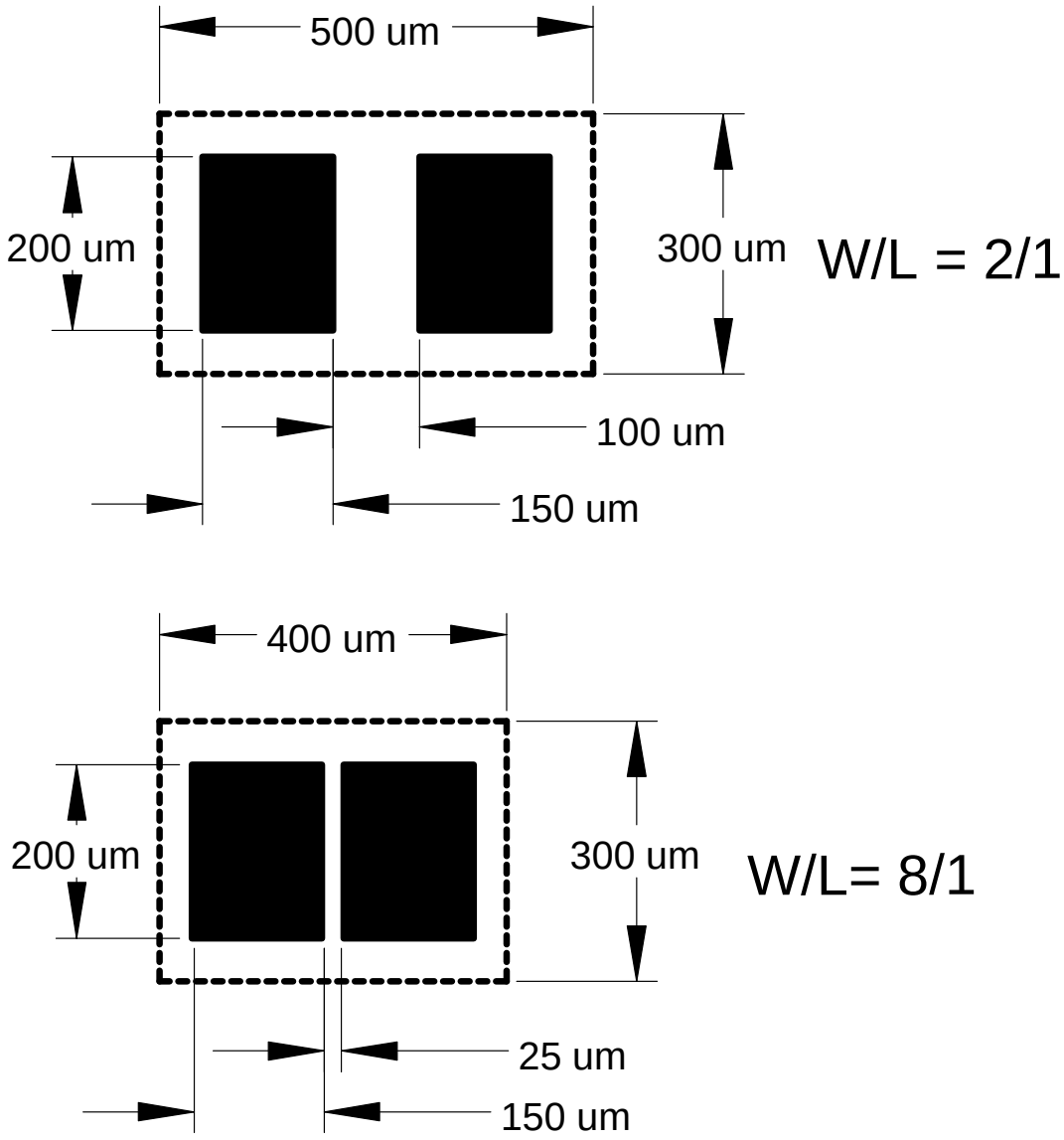

Figure 3.6: A diagram and relevant dimensions of mask #1 and mask #2 shown for W/L = 2/1 and W/L = 8/1. Mask #1, the mask for the body islands, is shown with the dotted lines and mask #2, the mask for the source and drain area, is shown as the black fill.

This recipe is qualified for critical dimensions as small as 25 μm, on a glass substrate, but if a different mask or a smaller critical dimension is required, the process should be re-optimized for the new application.

3.3 Characterization

3.3.1 Electrical Characterization

Electrically measuring devices with critical dimensions < 100 μm requires special techniques and equipment. Electrical contact to TTFT devices made via photolithography is accomplished using a microprobe station. A microprobe station consists of finely pointed probes, ~ 10 μm in diameter, mounted on micromanipulators, a chuck for holding the substrate, and a microscope for viewing the probes and substrate. Typically, a microprobe station is equipped with a parameter analyzer for measuring DC I-V curves, and a C-V meter for measuring capacitance.

Obtaining consistent ohmic electrical contact between the probes and the device under test is often a source of difficulty. It is essential that both the contact surface and probe tips are clean and that sufficient and consistent pressure is applied at each tip. Probe tip pressure is set by the scrub length, *i.e.* the length which the probe tips move across the contact surface after contact. Too small a scrub length and the pressure will be insufficient to make ohmic contact. Too large a scrub length and the device, probe tip, or both will be damaged. Aluminum makes an ideal contact material since the probe can be pressed into this soft metal, thus creating a clean contact. However, with careful application of probe tip pressure, the ITO contacts of TTFT devices are also adequate. Electrical characteristics indicating

high source and drain resistance should be verified with different tip scrub lengths and fresh probe tips to eliminate the possibility of bad probing.

A new TTFT often does not perform the same as it does after a brief break in period. This is likely due to persistent photoconductivity, static charge, and/or gate insulator instabilities. Typically, before TTFT electrical characterization the gate voltage is set to an on voltage, typically 40 V, and the drain voltage is cycled, typically 0 to 40 V, until the drain current stabilizes. The drain voltage is then cycled again with the gate at 0 V. This seems to insure that the TTFT electrical characteristics are truly stable and minimizes the chances of measuring transient affects. Additionally, measurement should be performed in a dark box to minimize the effects of persistent photoconductivity.

Initial transistor characterization is accomplished by plotting the drain current (I_D) versus drain voltage ($I_D - V_{DS}$) curves, at various gate voltages (V_{GS}) and an $I_D - V_{GS}$ curve at various drain voltages (V_{DS}) for a particular transistor, as shown in Figs. 3.7 and 3.8. $I_D - V_{DS}$ curves of a TTFT show whether the transistor is working properly; since whether the transistor has linear current characteristics at low V_{DS} and whether saturation occurs as the square of V_{GS} is apparent. $I_D - V_{GS}$ curves of a TTFT gives a qualitative idea of the threshold voltage and any instabilities in threshold voltage may be observed with this curve.

The current-voltage characteristics of an ideal MOSFET are modelled by the ideal triode region equation,

$$I_D = \mu C_i \frac{W}{L}(V_{GS} - V_T - \frac{1}{2}V_{DS})V_{DS}, \tag{3.1}$$

which is valid for $V_{DS} \leq (V_{GS} - V_T)$ and the ideal saturation region equation

$$I_D = \frac{1}{2}\mu C_i \frac{W}{L}(V_{GS} - V_T)^2, \tag{3.2}$$

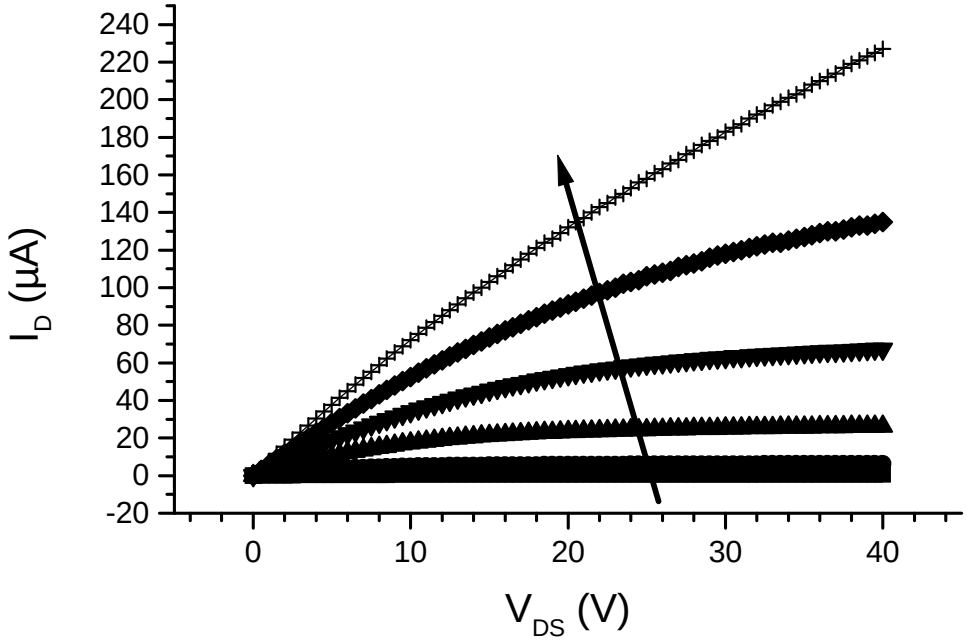

Figure 3.7: Representative $I_D - V_{DS}$ curves. Curves are shown for V_{GS} increasing from -10 to 40 V in 10 V increments, as indicated by an arrow.

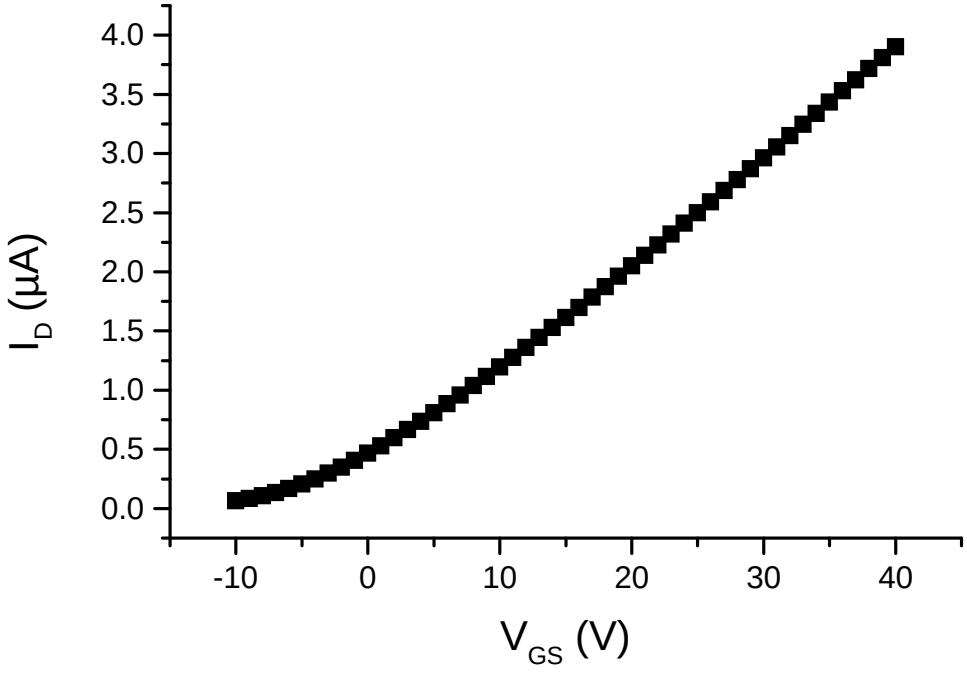

Figure 3.8: Representative linear region $I_D - V_{GS}$, $V_{DS} = 0.5\ V$, and saturation region $I_D^{1/2} - V_{GS}$, $V_{DS} = V_{GS}$, curves.

which is valid for $V_{DS} \geq (V_{GS} - V_T)$ where μ is the channel mobility, C_i is the gate insulator capacitance per unit area, W is the channel width, L is the channel length, and V_T is the threshold voltage. [68] Using Eqs. 3.1, 3.2, and the $I_D - V_{DS}$ and $I_D - V_{GS}$ current-voltage characteristic the parameters μ and V_T may be extracted.

Mobility may be extracted in one of three ways: effective mobility (μ_{eff}), field-effect mobility (μ_{FE}), and saturation mobility (μ_{sat}), as discussed in subsequent paragraphs. [108] Care must be take when comparing mobilities from different extraction methods since mobility may vary significantly from one method to the next. Additionally, channel mobility varies with field so that the bias point at which the calculation is made must be considered.

μ_{eff} is derived from the drain conductance (g_d) in the linear region [*i.e.* $V_{DS} \ll (V_{GS} - V_T)$], where

$$g_d = \frac{\partial I_D}{\partial V_{DS}} \mid_{V_{GS}=constant} . \tag{3.3}$$

For $V_{DS} \ll (V_{GS} - V_T)$ the drain conductance becomes,

$$g_d \approx \mu_{eff} C_i \frac{W}{L} (V_{GS} - V_T) \tag{3.4}$$

and thus,

$$\mu_{eff} \approx \frac{g_d L}{C_i W (V_{GS} - V_T)}. \tag{3.5}$$

The drawback of the effective mobility method is that V_T must be precisely known in order to calculate μ_{eff}. Often it is difficult to unambiguously define V_T, and this is particularly true of ZnO TTFTs. Additionally, the existence of source and drain resistance modifies the drain conductance so that it becomes

$$g_d(R_S) = \frac{g_{d0}}{1 + 2R_S g_{d0}}, \tag{3.6}$$

where g_{d0} is the drain conductance without source and drain resistance; Eq. 3.6 assumes the that the source (R_S) and drain resistance are equal. For large source and drain resistance, the effective channel mobility is underestimated.

The field-effect mobility (μ_{FE}) is calculated from the transconductance in the linear region [*i.e.* $V_{DS} \ll (V_{GS} - V_T)$], where

$$g_m = \frac{\partial I_D}{\partial V_{GS}} \mid_{V_{DS}=constant} . \tag{3.7}$$

Thus, in the linear region g_m may be expressed as,

$$g_m = \mu_{FE} C_i \frac{W}{L} V_{DS}, \tag{3.8}$$

thus yielding,

$$\mu_{FE} = \frac{L g_m}{C_i W V_{DS}}. \tag{3.9}$$

By calculating the field-effect mobility at a small drain current it is possible to minimize the effect of R_S. However, the calculation of μ_{FE} neglects the fact that mobility is strongly dependent on V_{GS}, and thus underestimates mobility compared to μ_{eff}.

The saturation mobility is calculated from the saturation current by,

$$\mu_{sat} = \frac{2Lm^2}{WC_i}, \tag{3.10}$$

where m is the slope of a plot of $I_{Dsat}^{1/2}$ versus $(V_{GS} - V_T)$. Saturation mobility also neglects the mobility dependence on V_{GS} and thus underestimates the actual mobility. Also, additional uncertainties may be caused by R_S. R_S causes the slope of $I_{Dsat}^{1/2}$ versus $(V_{GS} - V_T)$ to be reduced, thus further underestimating the mobility.

The threshold voltage, V_T, is defined as the voltage at which the channel begins to conduct charge. In the case of MOSFETs the threshold voltage is defined as the onset of strong inversion. A TTFT, however, is an accumulation-mode device, so that the threshold voltage is defined at the onset of strong accumulation. The threshold voltage may be determined by extrapolating an I_{DS} versus V_{GS} curve back to $I_{DS} = 0$ for small V_{DS}, *i.e.* in the linear region. [108] Since the slope of the

curve tends to vary with V_{GS}, the slope at the maximum g_m is typically used for extrapolation. An alternative method may be used for the estimation of V_T from an $I_{DS}^{1/2}$ versus V_{GS} curve in the saturation region. [108] Saturation is assured by setting $V_{GS} = V_{DS}$. In this method, $I_{DS}^{1/2}$ is extrapolated to zero in order to estimate V_T.

In addition to causing problems in the extraction of transistor parameters, a large source and drain resistance distorts the $I_D - V_{DS}$ characteristics of a transistor. First, consider the drain current in the triode region with the source and drain resistance included,

$$I_D = \mu C_i \frac{W}{L}(V_{GS} - V_T - \frac{1}{2}V_{DS})(V_{DS} - 2I_D R_S), \tag{3.11}$$

where the source and drain resistance are assumed to be equal. As long as the drain current, source resistance, or both are small, the drain current follows the ideal current characteristics given in Eq. 3.1. In the saturation region, the drain current becomes

$$I_D = \frac{1}{2}\mu C_i \frac{W}{L}(V_{GS} - I_D R_S - V_T)^2, \tag{3.12}$$

with the source and drain resistance included. Thus, when the source resistance is large, a negative feedback results that limits the saturation current. When I_D stops increasing as V_{GS} is increased, is traditionally referred to as "current-crowding," and is indicative of the presence of an unacceptably large source resistance. [109] Since this terminology is often confused with current-crowding related to contact resistance this behavior will be referred to as "I_D current limiting" in this dissertation.

3.3.2 Visual Observation and Optical Microscopy

Simple visual inspection of a thin-film is often very useful in trouble-shooting films problems. Unfortunately, visual inspection is often discounted as a viable diag-

nostic tool since it provides only a qualitative assessment of a thin-film. Qualitative information such as color, opacity, optical absorption, roughness, and thickness estimates are often obtainable from a visual observation.

Optical light microscopy is also a useful method for assessing thin-films properties. Information about gross physical defects such as delamination, particle contamination, large pinholes, and poor film coverage are easily and quickly obtained with the aid of an optical light microscope. However, the detail that may be resolved from an optical light microscope is limited by diffraction effects, so that other techniques must be used for the evaluation of physical features with dimensions less than $\sim 0.50\ \mu m$. [11]

3.3.3 Scanning Electron Microscopy (SEM)

When features smaller than $\sim 0.50\ \mu m$ are to be viewed, optical photons can no longer be used. SEM is often the method of choice for observations of linewidths as small as $10\ nm$. [11] Additionally, the depth of field is greater with an SEM than a light microscope for a given magnification.

SEM is accomplished by rastering an electron beam across a sample surface. Secondary electrons, in the energy range of 0–50 eV, are detected and used to modulate the intensity of a signal sent to a CRT display. The x and y coordinates of the CRT correspond to the position of the rastered beam, thus yielding an image. SEM images with a magnification up to 300,000$\times$ are possible.

3.3.4 Profilometery

Profilometery is a quick way to obtain thickness and geometry information about a thin-film. [110] With profilometry, a stylus is run along a film surface and

depth is measured by a piezoelectric sensor. Generally, the sharper and deeper the step, the more accurate the data. In theory, steps as small as $\sim 0.5\ nm$ may be measured, although vibration typically limits accuracy to $\sim$5–10 nm.

3.3.5 X-Ray Diffraction (XRD)

XRD is a useful method for assessing the characteristics of a crystal. [111] XRD is a well developed experimental methodology, so only a brief explanation of the methods relevant to this dissertation are discussed here. XRD is based on the Bragg law which governs the scattering angle at which constructive interference occurs. Constructive interference occurs at

$$\lambda = 2d\sin(\theta), \tag{3.13}$$

where λ is the incident x-ray wavelength, d is the crystal plane lattice spacing, and θ is the scattering angle, as shown in Fig. 3.9. Typically XRD data is shown as a plot of the x-ray intensity versus the scattering angle, an example of which is shown in Fig. 3.10. Peaks occur where the Bragg equation is satisfied. By comparing the measured XRD peaks to a calculated standard, the prominent crystal orientations and particle size may be determined.

3.3.6 Atomic Force Microscopy (AFM)

Atomic force microscopy (AFM) is a method of precisely imaging a thin-film surface. [112]. An AFM system consists of a scanner capable of motion in X, Y, and Z directions and which is attached to a fine probe tip. The tip contact pressure is measured by a piezoelectric sensor and a deflection angle is measured by laser light intensity which bounces off of a cantilever which is attached to the tip.

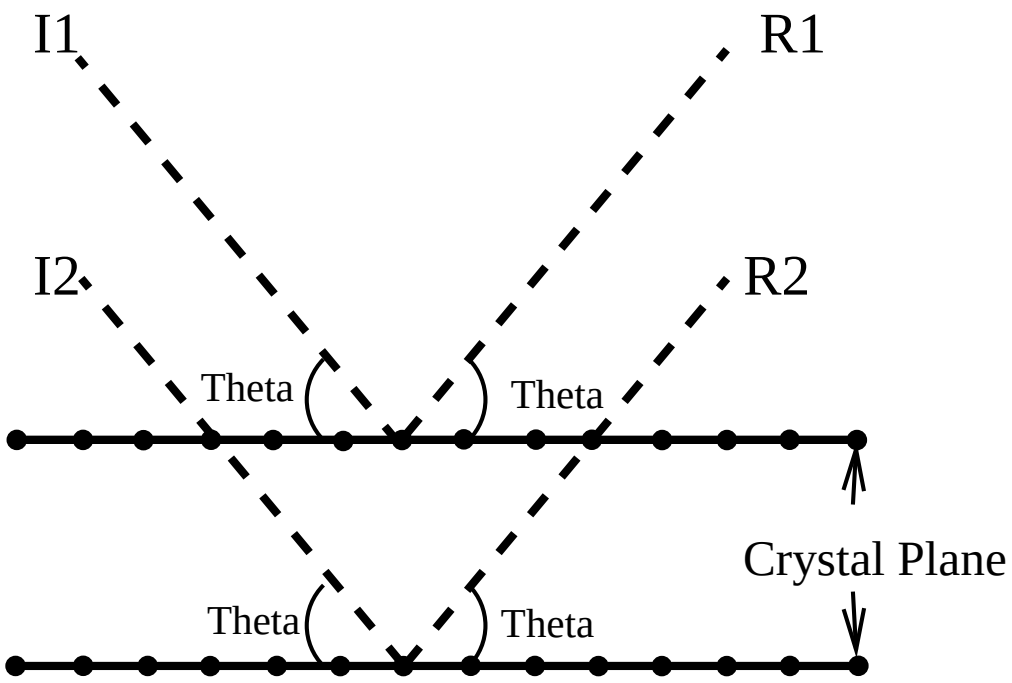

Figure 3.9: An illustration of the Bragg scattering angle (θ) in relation to a crystal plane, the incident (I1 and I2) x-ray beam, and the reflected (R1 and R2) x-ray beam.

An AFM may be operated in a contact, tapping, or non-contact mode. In the contact mode the tip passes across the sample surface with a constant applied force, resulting in a high throughput and good tracking on rough surfaces. However, a combination of high normal and lateral forces may distort and damage the sample surface. The tapping mode almost completely eliminates the lateral force by tapping the probe tip against the sample surface at a constant frequency as a scan is performed. Additionally, lateral resolution is often improved in the tapping mode, but the maximum scan speed is slower. When the sample surface cannot tolerate any tip contact, the non-contact mode may be employed. The probe tip is oscillated near the sample surface by van der Waal force sensing. However, the non-contact mode scan speed is slower than that of the contact and tapping modes. Also, the

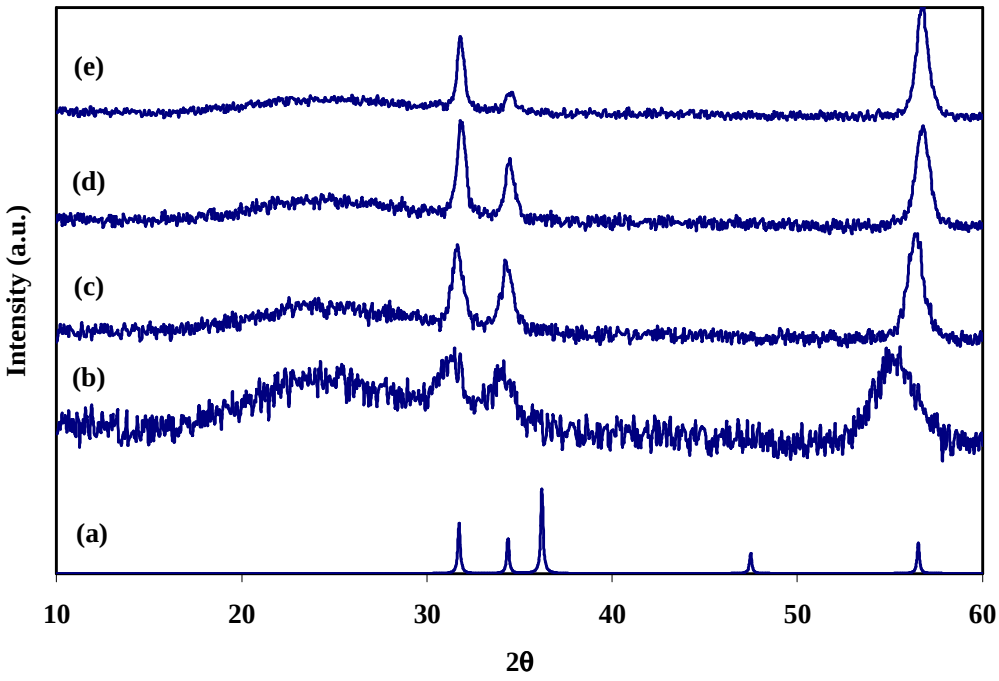

Figure 3.10: Sample XRD curves of an ion-beam sputtered ZnO thin-film on a glass substrate. Curves are shown for various annealing conditions: a) a calculated curve, b) as deposited, c) 300°C oxygen RTA, d) 500°C oxygen RTA, and e) 700°C oxygen RTA. [113]

lateral resolution is poor and only certain samples work well with the non-contact mode.

AFM data is often used to calculate the root-mean-square (RMS) roughness, estimated substrate depth, and grain size for a thin-film. The RMS roughness is defined as

$$RMS = \sqrt{\frac{\sum_{i=1}^{N}(x_i - x_\mu)^2}{N}}, \tag{3.14}$$

where x_μ is the mean surface height, x_i is the the surface height at data point i, and N is the total number of data points. The estimated substrate depth is given by

$$depth = x_m - x_{min}, \tag{3.15}$$

where x_{min} is the data point with the smallest value and x_m is the mode of the data set. The estimated substrate depth may perhaps be better described as the maximum pore depth as measured from an estimated surface to the lowest data point. The grain size is simply the average feature size.

4. THIN-FILM RESULTS

4.1 Spin-Coated Phosphors

Spin-coating deposition for this dissertation began as a means of synthesizing phosphor thin-films. Thus, the initial materials investigated are sulfides. This investigation was motivated by an interest in developing phosphors for alternating-current thin-film electroluminescent (ACTFEL) devices and for electron trapping materials (ETMs). [115, 116]

Exploration of spin-coating solutions involving Sr and Mg cations led to important insights applicable to spin solution development, related to the following topics: substrate cleaning, solution filtering, solvent choice, the use of glycine, and boiling. The importance of substrate cleaning and preparation is discussed in Sec. 3.1.1. Solution filtering produced consistently better results than with the unfiltered solution since it is difficult to produce a spin solution free of insoluble contamination. A 0.4 μm mesh filter is found to work very well for removing particle contamination prior to spin-coating.

4.1.1 Spin-Coating SrS

A number of solvents used in conjunction strontium nitrate are explored including deionized water, a mixture of ethylene glycol and deionized water, a mixture of methanol and deionized water, a mixture of acetic acid and deionized water, and a mixture of ethanol and deionized water. Deionized water, the mixture of methanol and deionized water, and the mixture of acetic acid and deionized water resulted

in films with incomplete coverage, as discussed in Sec. 3.1.2.1. This may be due, in part, to the fact that substrate cleaning methods were not perfected at the time that these experiments were performed, but it is likely also related to poor adhesion between the substrate and spin-coating solution. Mixed ethylene glycol and deionized water spin solutions tend to spin-coat well, but poor film uniformity results during the solvent bake due to the low vapor pressure of ethylene glycol. Ethanol and deionized water spin solutions yield consistently good quality thin-film coatings and produces good SrS films after the conversion bake. Thus, mixed ethanol and deionized water is used as the solvent in all subsequent strontium nitrate-based spin solution development.

Spin-coated strontium nitrate films are converted directly to SrS by baking in an H_2S gas flow for $\sim 1.5\ hrs$. Typically, spin-coated SrS films from strontium nitrate are 150–500 nm thick. Doping is accomplished by source-layer diffusion-doping using $CuCl_2$ or $EuCl_3$ as the Cu or Eu luminescent impurity source. Phosphors are qualitatively tested for photoluminescences (PL) using a UV lamp in a darkened room. Additionally, the conversion from strontium nitrate to SrS is verified with XRD.

Spin-coated phosphor development at Oregon Sate University is plagued by contamination problems. Almost invariably "undoped" films produced green PL, presumably from Cu contamination. Typically, the contamination-induced PL is nonuniform across the substrate, with substrate edges typically producing brighter PL than the center. It is likely that the contamination is introduced during the sulfidization step. Spin solution contamination would be homogeneous throughout the spin-coated film, but contamination introduced during a furnace bake would likely diffuse in from the furnace tube or crucible producing nonuniform PL across the substrate.

Dim electroluminescence is achieved from spin-coated SrS:Eu in an ACTFEL structure, as shown in Fig. 4.1. The strontium nitrate solution is spun directly onto an ultrasonically cleaned ITO/ATO-coated glass substrate. Typically, ACTFEL devices are constructed with two insulators, one insulator at either electrode. The ACTFEL structure used for testing spin-coated SrS, however, has only one insulator. In addition the phosphor layer for the spin-coated ACTFEL device is only $\sim 150\ nm$ thick; ACTFEL phosphor layers are typically $\sim 500\ nm$ thick. Based on lessons learned from later spin solution development, dramatic improvements in spin-coated ACTFEL performance should be possible with structure optimization, dopant optimization, and improvements in H_2S conversion procedure. However, for the purposes of this dissertation the liquid-phase phosphor development is primarily of interest for the lessons learned about spin-coating, that are later applied to zinc nitrate-based spin solution development.

4.1.2 Spin-Coating MgS

Spin-coating a magnesium nitrate in ethanol mixed with deionized water solution results in crystallization, as discussed in Sec. 3.1.2.4. However, a spin solvent of ethanol and deionized water did not result in crystallization with the large cation strontium nitrate. Adding glycine to a magnesium nitrate deionized water solution effectively inhibits crystallization. Also, boiling magnesium nitrate, glycine, and deionized water solutions leads to gelling. This gelling is effective at improving adhesion between the spin solution and substrate, and also increases the solution viscosity. Adding ammonia to the spin solution has a similar effect to boiling, but sometimes leads to too much solution gelling over time, *i.e.* the solution become too viscous for spin-coating.

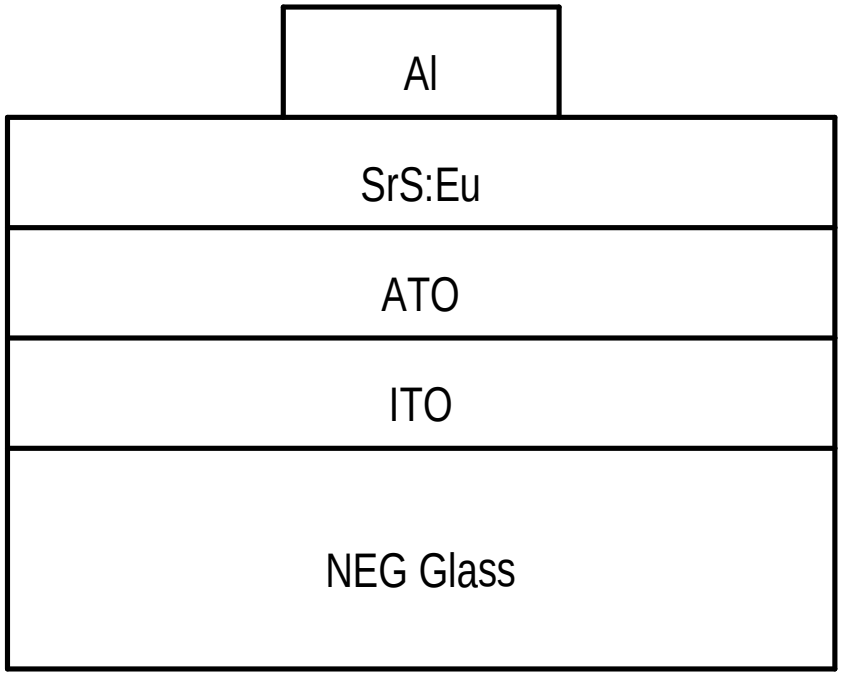

Figure 4.1: Structure of a single insulator spin-coated SrS:Eu ACTFEL device.

Spin-coated magnesium nitrate thin-films are first converted to MgO via a high temperature ($\sim 600°C$) air bake prior to sulfidizaton. Sulfidizaton of MgO is accomplished by baking at $770°C$ for 2 hrs under a flow of CS_2 gas. CS_2 sulfudization is a strong conversion conditions and is not a good manufacturing process. The resulting MgS films exhibit some PL, but Cu contamination problems precluded further development.

4.2 ZnO Via Spin-Coating

4.2.1 Process Development

4.2.1.1 ZnO Spin Solution Development

The lessons learned from spin-coated MgS development are directly applicable to ZnO spin solution development for ZnO TTFT applications. Zinc and magnesium nitrate behave similarly in terms of spin solution development since both Mg and Zn are relatively small cations. Strontium nitrate, with a relatively large Sr cation, does not tend to crystallize as the solvent evaporates from the nitrate thin-film. In contrast, both magnesium and zinc nitrate thin-films tend to crystallize.

Zinc nitrate, like magnesium nitrate, tends to crystallize in a hexagonal pattern after spin-coating; the addition of glycine to the spin solution is very effective at preventing crystallization. Additionally, boiling a zinc nitrate solution with glycine leads to gelling, thus further improving the spin solution properties.

4.2.1.2 Sputtered ZnO thin-films

When developing a new deposition method it is important to be cognizant of the characteristics of existing deposition methods so that the advantages and disadvantages of the new method may be discerned. Additionally, comparing different methods of depositing the same material provides a means for extracting deposition properties from materials properties. For thin-film analysis in this dissertation ion-beam and RF sputter deposited ZnO is used as a standard to compare to spin-

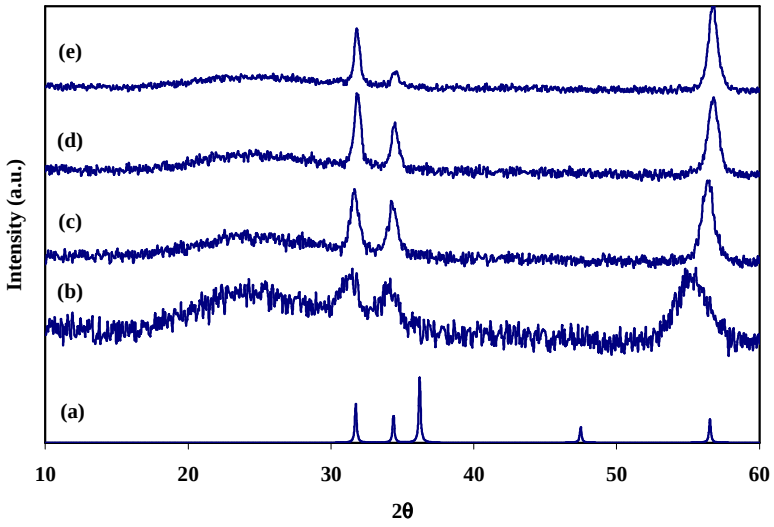

Figure 4.2: XRD patterns of ion-beam sputtered ZnO. (a) Simulated XRD for ZnO, (b) ZnO film as deposited, (c) ZnO film RTAed at $300°C$ in O_2, (d) ZnO film RTAed at $500°C$ in O_2, and (e) ZnO film RTAed at $700°C$ in O_2. [113]

coated ZnO. Sputtering is ubiquitously used in the thin-film industry, and is thus an appropriate standard for comparison.

Ion-beam sputtering has been used to produce well oriented (002) ZnO thin-films. [36] However, the ion-beam sputtered ZnO deposited at Oregon State University to date is grown on an unheated substrate so that the crystal orientation of the resulting thin-film is randomly oriented, as shown in Fig. 4.2. Although the XRD peaks of ion-beam sputtered ZnO sharpen after a post-deposition anneal, a dominant peak indicating a preferred orientation is not present.

RF sputtered ZnO from Oregon State University has a strong preferred orientation along the (103) axis. Typically ZnO tends to show a preferred orientation along the (002) axis, so it is interesting that this RF sputtered ZnO has a preferred orientation along the (103) axis. SEM images of RF sputtered ZnO films show a dense high quality film, as indicated in Fig. 4.4.

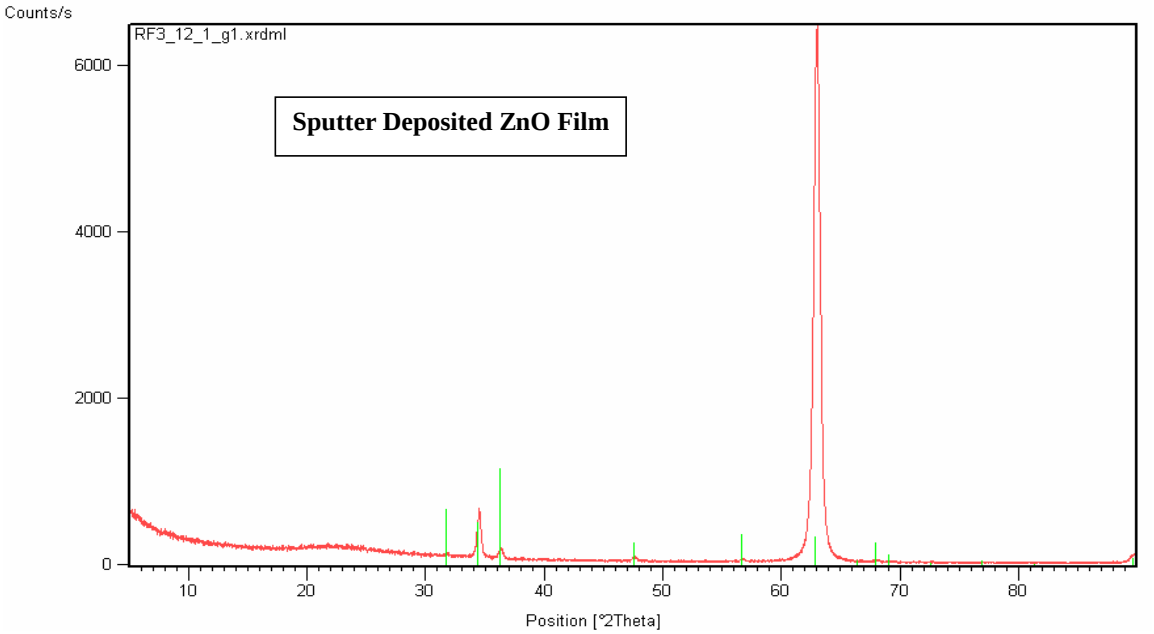

Figure 4.3: An XRD pattern of an RF sputtered ZnO thin-film on Corning^{TM} 1737 glass. Notice the large (103) peak. [114]

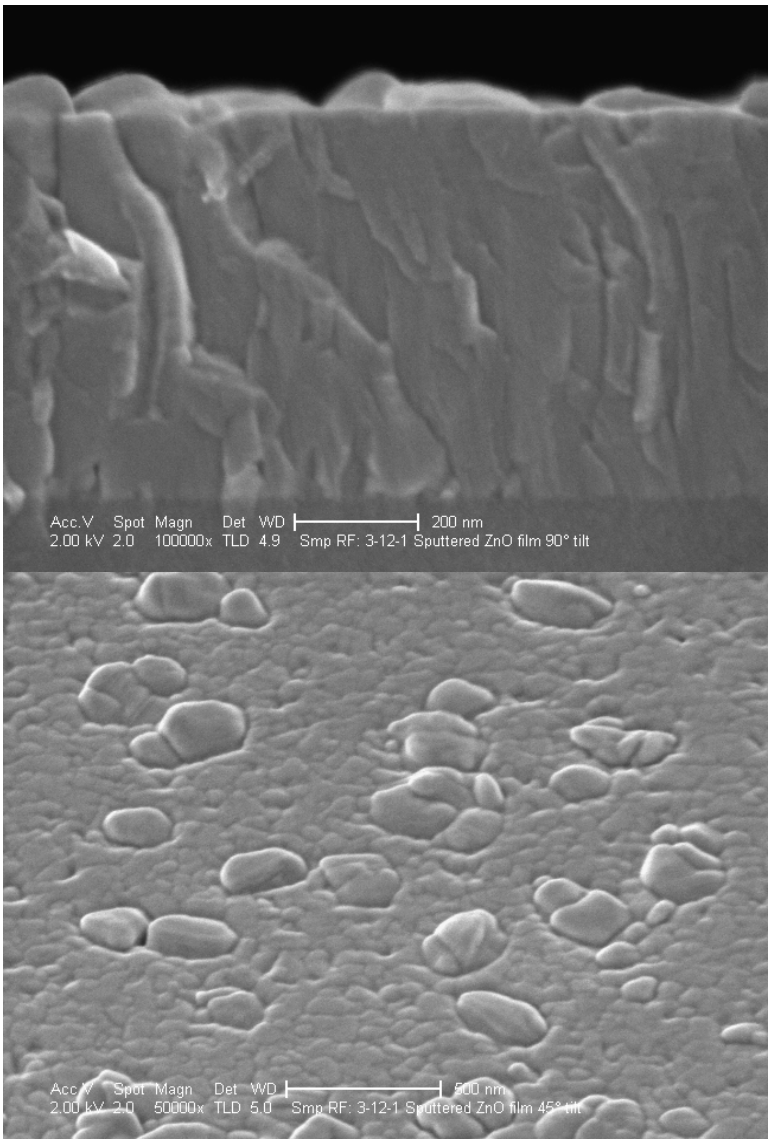

Figure 4.4: A side- and top-view SEM image of an RF sputtered ZnO film on a Corning^{TM} 1737 glass with a 200 nm and 500 nm scale, respectively. [114]

4.2.1.3 Spin-Coated ZnO Annealing

Thermal cycling of spin-coated thin-films plays an important role in establishing the density, crystal orientation, and degree of conversion of the final ZnO film. The thermal cycling experiment presented herein is based on the hypothesis that three heating cycles are necessary to fully convert the spin-coated zinc nitrate gel to ZnO. First, a low-temperature bake, *i.e.* solvent bake, to drive out any solvent remaining after the spin deposition is used. Next, a medium-temperature bake, *i.e.* a pre-bake, is employed to slowly burn-off the glycine stabilizer/thickener and to begin to convert the zinc nitrate gel to ZnO. Finally, a high-temperature furnace anneal or RTA, *i.e.* the final bake, completes the conversion to ZnO and insures maximum crystallinity.

Table 4.1 summarizes relevant SEM and XRD results, along with their relevant processing parameters and the grain size. The grain size is calculated from the XRD peak width. All films are spin-coated at 3000 rpm for 15 sec, followed by a 500 rpm spin for 30 sec to aid in removing any excess solvent. Later experiments indicated that the 500 rpm spin is not necessary and a 3000 rpm spin for 30 sec is adequate.

The bake parameters for the final bake experiment are: (i) a solvent bake in a convection oven at 140°C in air for $\sim$ 30 min, (ii) a pre-bake on a hot plate at 260°C in air for 2 hrs, and (iii) a final RTA bake at 600°C, 500°C, or 400°C in O_2 or an oven bake at 400°C for 2 hrs in an air furnace. These parameters are established primarily through trial-and-error, empirical studies, and the ZnO spin-coating literature for zinc acetate solutions, as discussed in Sec. 2.4.4.

SEM images for the 600°C and 500°C final bake are very similar, as indicated in Figs. 4.5 and 4.6. Notice that these thin-films are highly porous and are comprised of loosely packed grains. The grain sizes apparent in the SEM images, as observed

Table 4.1: A summary of processing parameters and grain sizes for various spin-coated ZnO thin-films. §indicates convection oven annealing, †indicates furnace annealing, and ‡indicates hot plate annealing.

SEM Fig.	XRD Fig.	Solvent Bake	Pre-Bake	Final Bake	XRD Grain Size (nm)
4.5	4.9	140°C air§	260°C air (2 hrs)‡	RTA 600°C O_2	17.5 ± 1.5
4.6	4.9	140°C air§	260°C air (2 hrs)‡	RTA 500°C O_2	12.7 ± 1.3
4.7	4.9	140°C air§	260°C air (2 hrs)‡	RTA 400°C O_2	13.1 ± 2.2
4.8	4.9	140°C air§	260°C air (2 hrs)‡	400°C air (2 hrs)†	17.3 ± 1.5
4.10	4.13	N/A	600°C air (10 min)†	RTA 600°C O_2	25 ± 1.2
4.11	4.13	N/A	400°C air (10 min)†	RTA 600°C O_2	19 ± 2
4.12	4.13	N/A	300°C air (10 min)‡	RTA 600°C O_2	16.9 ± 1

in Figs. 4.5 and 4.6, closely match those calculated from the XRD patterns of 17.5 nm and 12.7 nm for the 600°C and 500°C final bake, respectively. Thus, there is only a slight improvement in grain size in going from a 500°C to a 600°C RTA.

The 400°C furnace anneal and 400°C RTA final bakes are very revealing about the nature of conversion from zinc nitrate/glycine to ZnO, as shown in Figs. 4.7 and 4.8. A 400°C RTA is not adequate to completely convert the zinc nitrate to ZnO, as apparent in the SEM shown in Fig. 4.7. Based on differences in appearance between the glass substrate, the unconverted zinc nitrate, and the ZnO, it is clear that the conversion begins at the zinc nitrate surface and progresses toward the substrate. If provided enough time, zinc nitrate completely converts to ZnO at 400°C, as apparent with the 2 hour furnace anneal shown in Fig. 4.8. At some temperature between 400°C and 500°C, the conversion process occurs much more rapidly since the film RTAed at 500°C is completely converted, while the film RTAed at 400°C is not. The 400°C furnace annealed film has a grain size of 17.3 nm which is almost as large as that of the 600°C RTA film (17.5 nm). However, cracking is severe for the furnace annealed film. The XRD pattern is extremely weak for the film RTAed at 400°C, since conversion is incomplete and there is very little crystallized ZnO to scatter the incoming X-rays.

The XRD curves for the final bake experiment are not especially revealing since there is not a preferred crystal orientation for any of the films measured, as indicated in Fig. 4.9. All curves possess the characteristic peaks of ZnO, as calculated. All four curves are very similar, except for the XRD pattern of the 400°C RTA, which is extremely weak.

Based on SEM and XRD results, the 600°C RTA produces the largest grain size of any of the final bake temperatures. Therefore, for subsequent experiments a 600°C RTA final bake is used. It is very likely that grain size and possibly

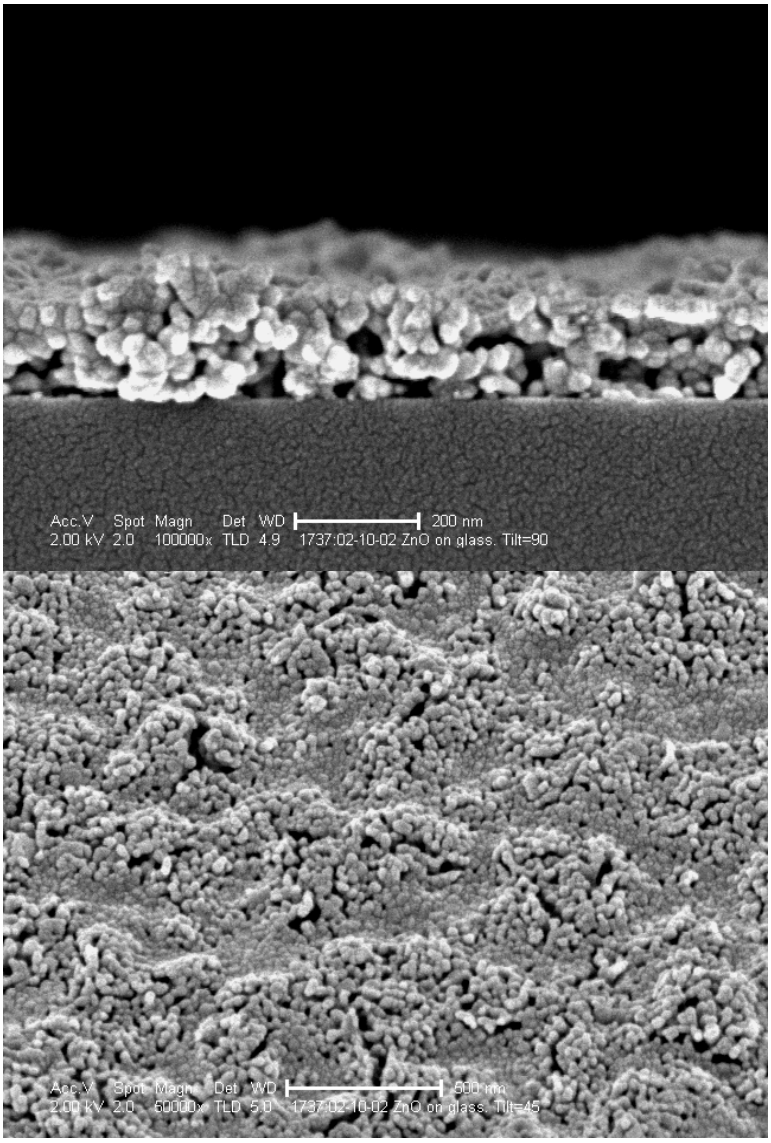

Figure 4.5: A side- and top-view SEM image with a 200 nm and 500 nm scale, respectively. These are images of a spin-coated ZnO film on a Corning^{TM} 1737 glass substrate. The thin-film is spin-coated from a zinc nitrate solution and the final bake is an RTA at 600°C in oxygen. [114] Notice that the grain size apparent in the top-view is $\sim 20 - 30$ nm.

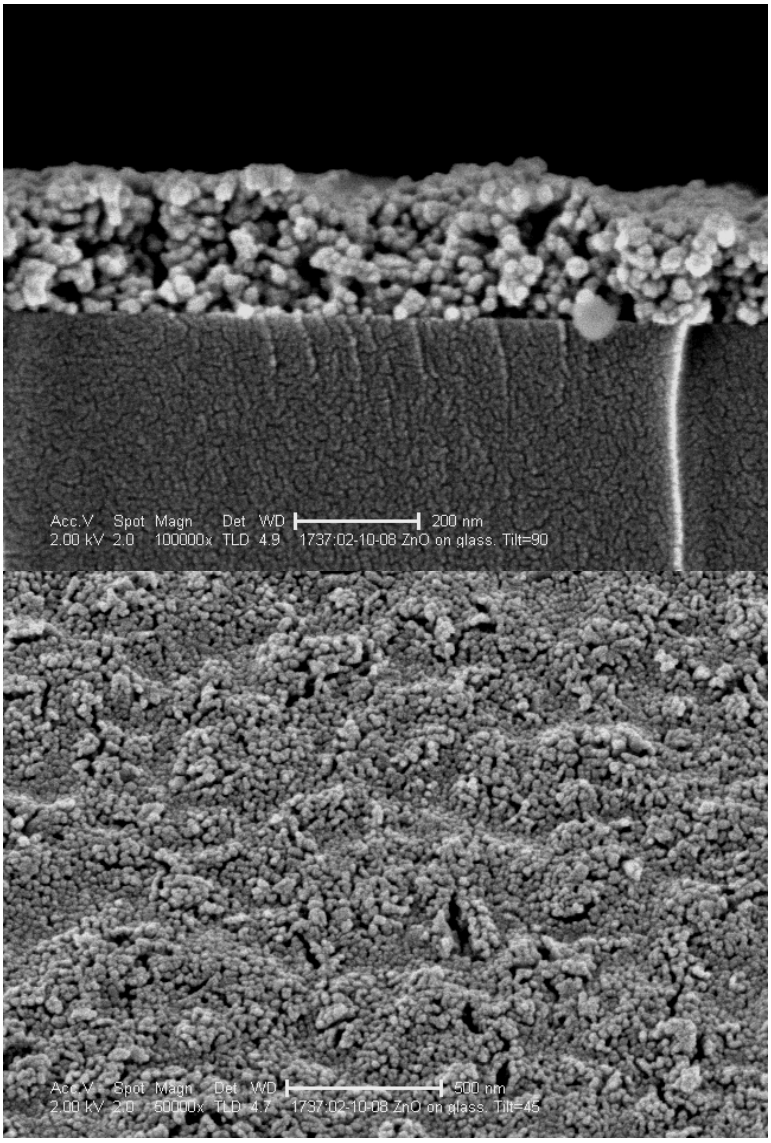

Figure 4.6: A side- and top-view SEM image with a 200 nm and 500 nm scale, respectively. These are images of a spin-coated ZnO film on a Corning^{TM} 1737 glass substrate. The thin-film is spin-coated from a zinc nitrate solution and the final bake is an RTA at 500°C in oxygen. [114] Notice that the grain size apparent in the top-view is $\sim 10 - 20$ nm.

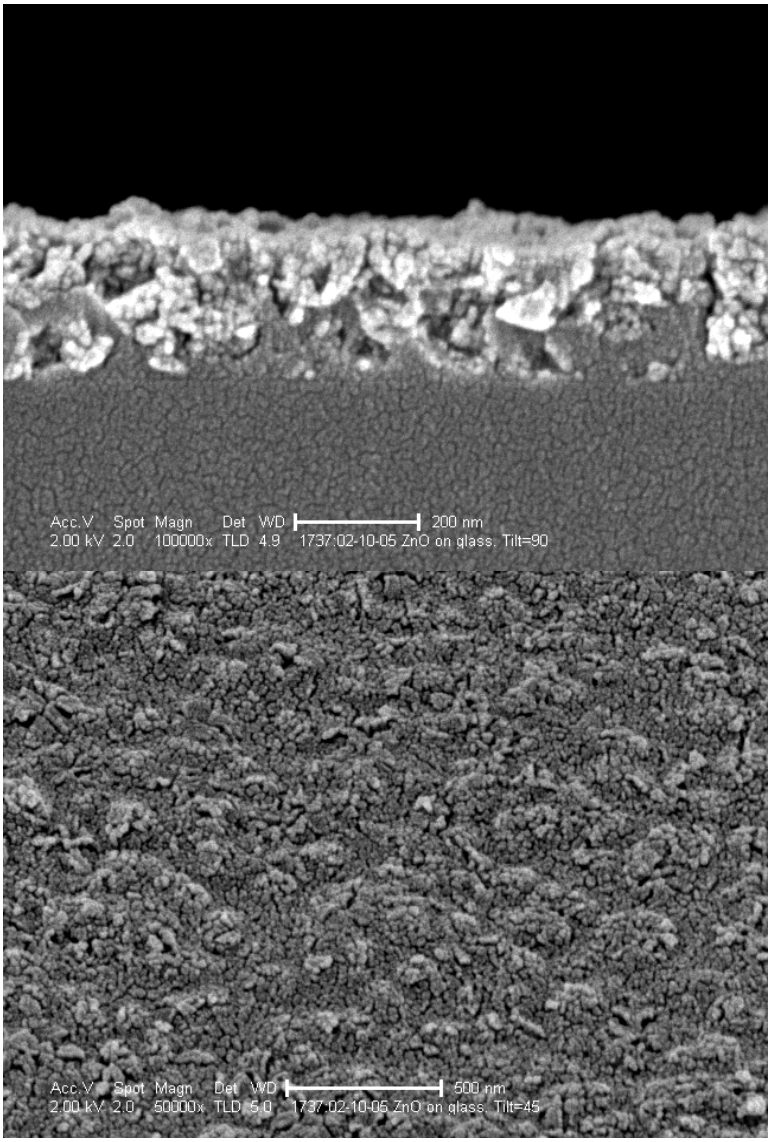

Figure 4.7: A side- and top-view SEM image with a 200 nm and 500 nm scale, respectively. These are images of a spin-coated ZnO film on a Corning^{TM} 1737 glass substrate. The thin-film is spin-coated from a zinc nitrate solution and the final bake is an RTA at 400$^{\circ}C$ in oxygen. [114]

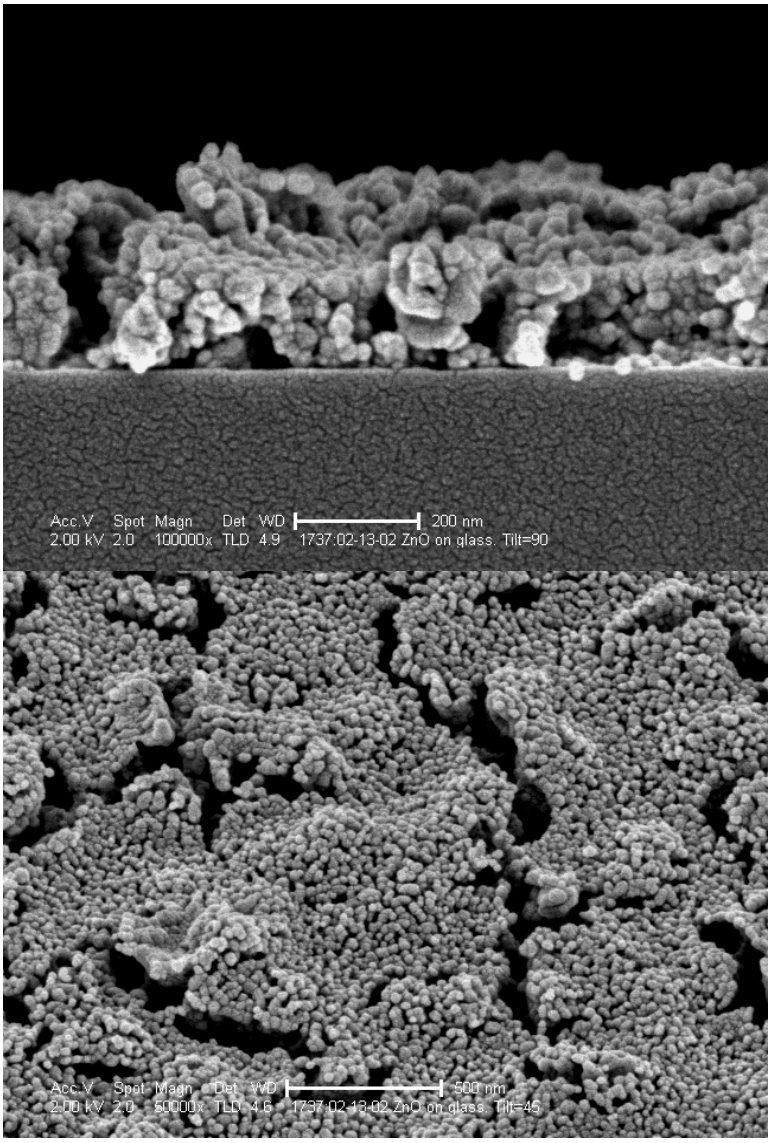

Figure 4.8: A side- and top-view SEM image with a 200 nm and 500 nm scale, respectively. These are images of a spin-coated ZnO film on a Corning^{TM} 1737 glass substrate. The thin-film is spin-coated from a zinc nitrate solution and the final bake is a furnace bake at 400°C in air for 2 hrs. [114] Notice that the grain size apparent in the top-view is $\sim 10 - 20$ nm.

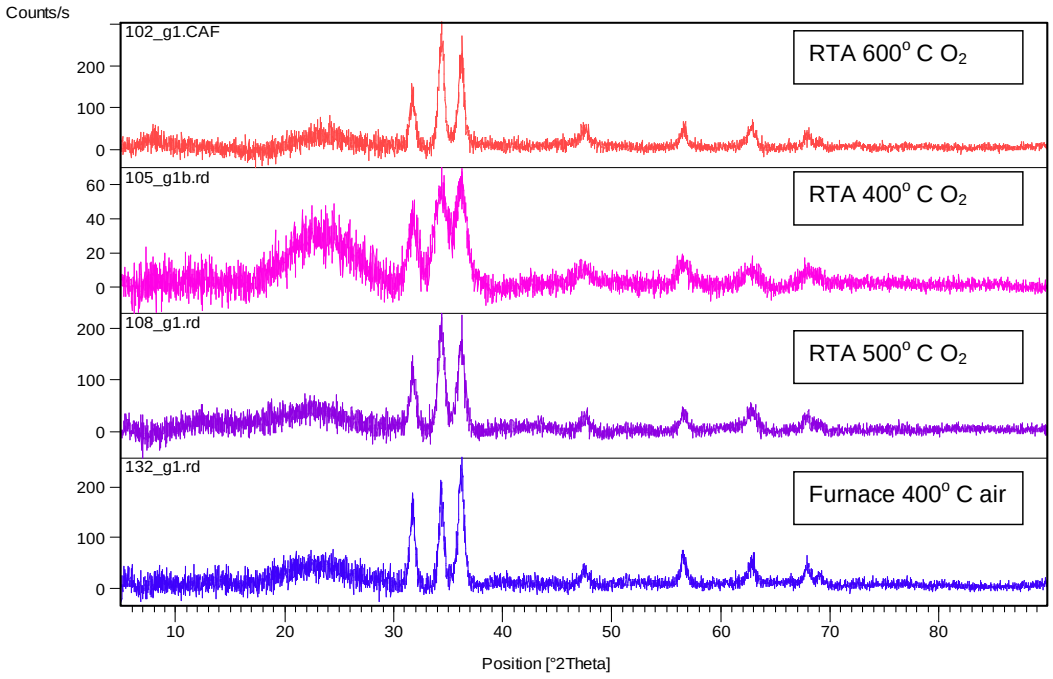

Figure 4.9: XRD patterns of spin-coated ZnO thin-films with different final bakes and which are deposited onto Corning^{TM} 1737 glass substrates. [114]

preferred crystal orientation would continue to improve for temperatures higher than 600°C; however many of the substrates used exhibit problems with delamination and warpage at temperatures above 600°C.

Pre-bake temperatures of 600°C, 400°C, 300°C are selected to cover a range of reasonable pre-bake temperatures. It is necessary, however, to use three different heating sources for each of the pre-bake steps due to equipment constraints and the need to keep every other processing step precisely the same. Two different air furnaces are used for the 600°C and 400°C pre-bakes and a hot plate is used for the 300°C pre-bake. Each thin-film is RTAed at 600°C in oxygen following the pre-bake. Even though the a 600°C RTA cycle is likely to have little effect on the film pre-baked at 600°C it is performed in order to keep the process follow consistent.

The $600°C$ pre-bake SEM image shows a surprisingly uniform and dense film, as indicated in Fig. 4.10. The XRD grain size is large (25 nm) and in close agreement with that observed in the SEM image. In addition, the $600°C$ pre-bake film does not have any cracks or large voids. Pores are visible in areas where the crystal grains have grown together.

The $400°C$ and $300°C$ pre-baked films appear to be very similar, as shown in Figs. 4.11 and 4.12. The XRD grain sizes (19 and 16.9 nm for $400°C$ and $300°C$, respectively) are also very similar and are in good agreement with the grain sizes apparent in the SEM images.

The XRD data is perhaps the most informative with regard to the pre-bake study, as shown in Fig. 4.13. The (002) peak increases in sharpness and prominence as the pre-bake temperature is increased from $300°C$ to $600°C$, indicating that ZnO films have a large grain size and become increasingly well oriented to the (002) plane as the pre-bake temperature is increased. The (002) peak from the $600°C$ pre-bake is certainly better oriented to the (002) plane than the ion-beam sputtered films shown in Fig. 4.2. Thus, when considering crystal orientation, the $600°C$ pre-bake film is at least as preferentially oriented, if not better oriented, than the ion-beam sputtered film.

The spin solution used to make the ZnO thin-films for the final bake experiment is slightly different than than the spin solution discussed in Sec. 3.1.4.1 and used in the pre-bake and ZnO TTFT experiments. For the spin solution use in the final bake experiment ammonia is mixed into the spin solution to gel it; however, for the spin solution discussed in Sec. 3.1.4.1 gelling is induced by boiling the spin solution. The $300°C$ pre-bake film is very similar to the film RTAed $600°C$ in the final bake study, verifying that the change in solution did not significantly change the film properties, as shown in Figs. 4.12 and 4.5, respectively. In addition, the

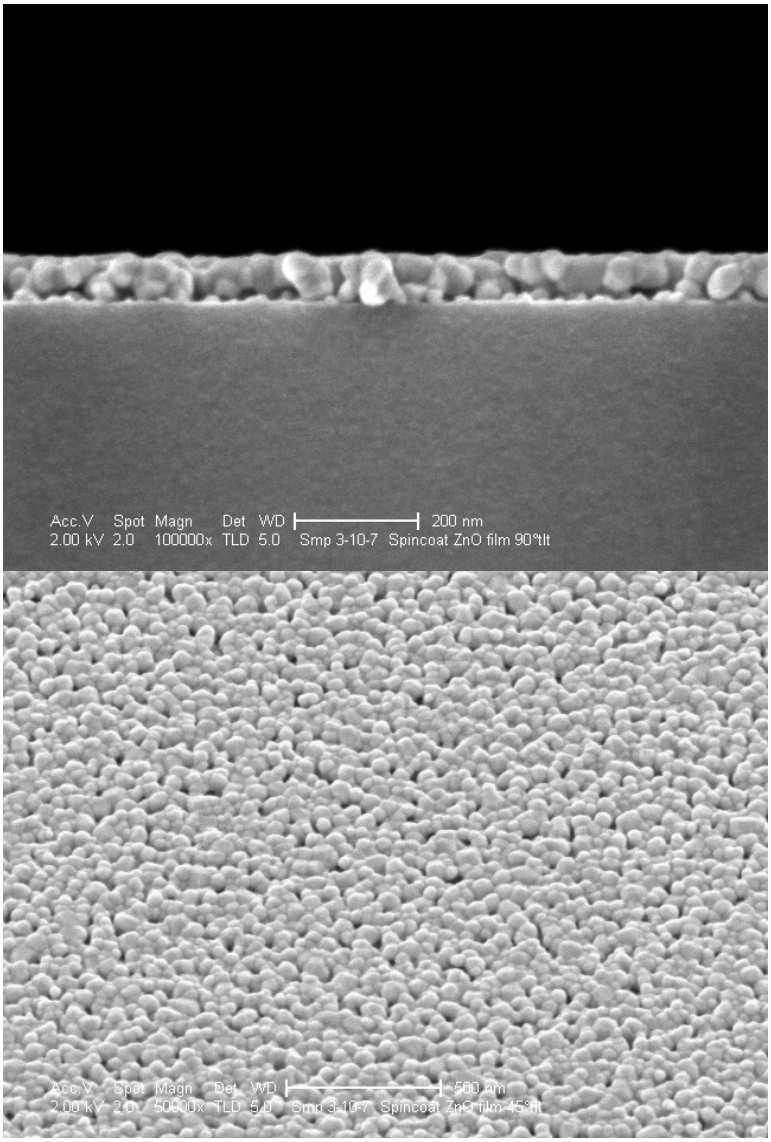

Figure 4.10: A side- and top-view SEM image with a 200 nm and 500 nm scale, respectively. These are images of a spin-coated ZnO film using a zinc nitrate spin solution pre-baked at $600°C$ in air on a Corning^{TM} 1737 glass substrate. [114] Notice that the grain size apparent in the top-view is $\sim 20 - 30$ nm.

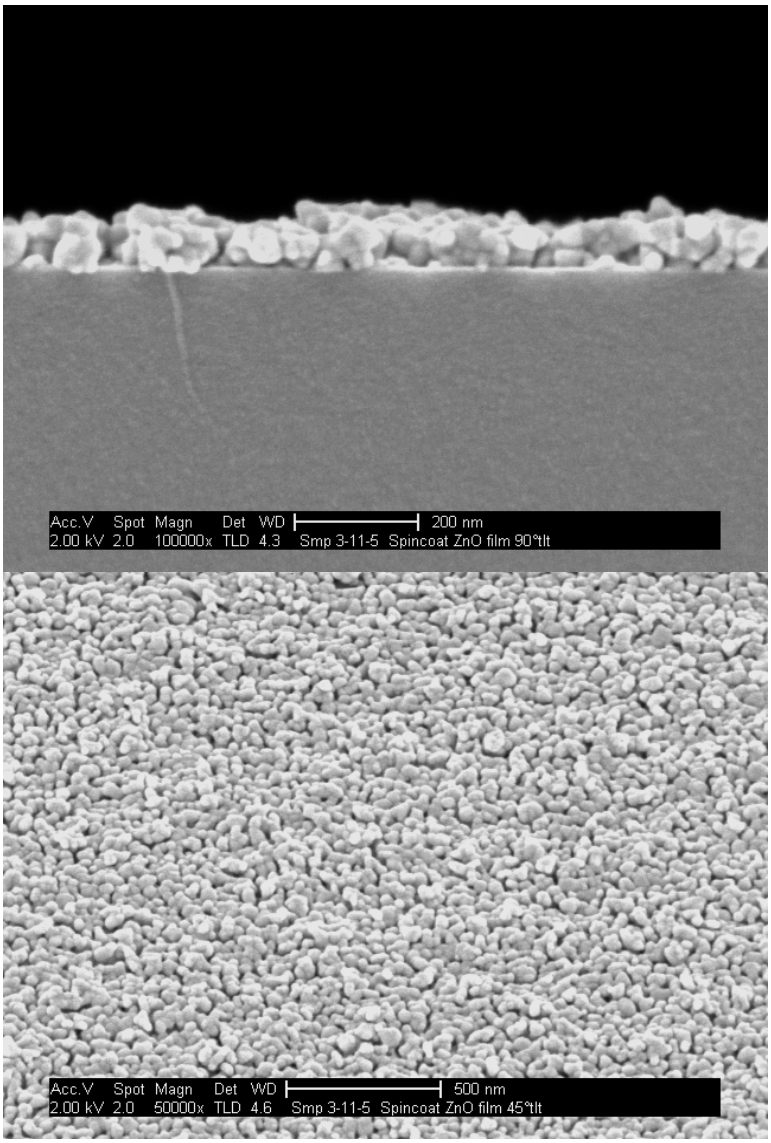

Figure 4.11: A side- and top-view SEM image with a 200 nm and 500 nm scale, respectively. These are images of a spin-coated ZnO film using a zinc nitrate spin solution pre-baked at $400°C$ in air on a Corning^{TM} 1737 glass substrate. [114] Notice that the grain size apparent in the top-view is $\sim 20 - 30$ nm.

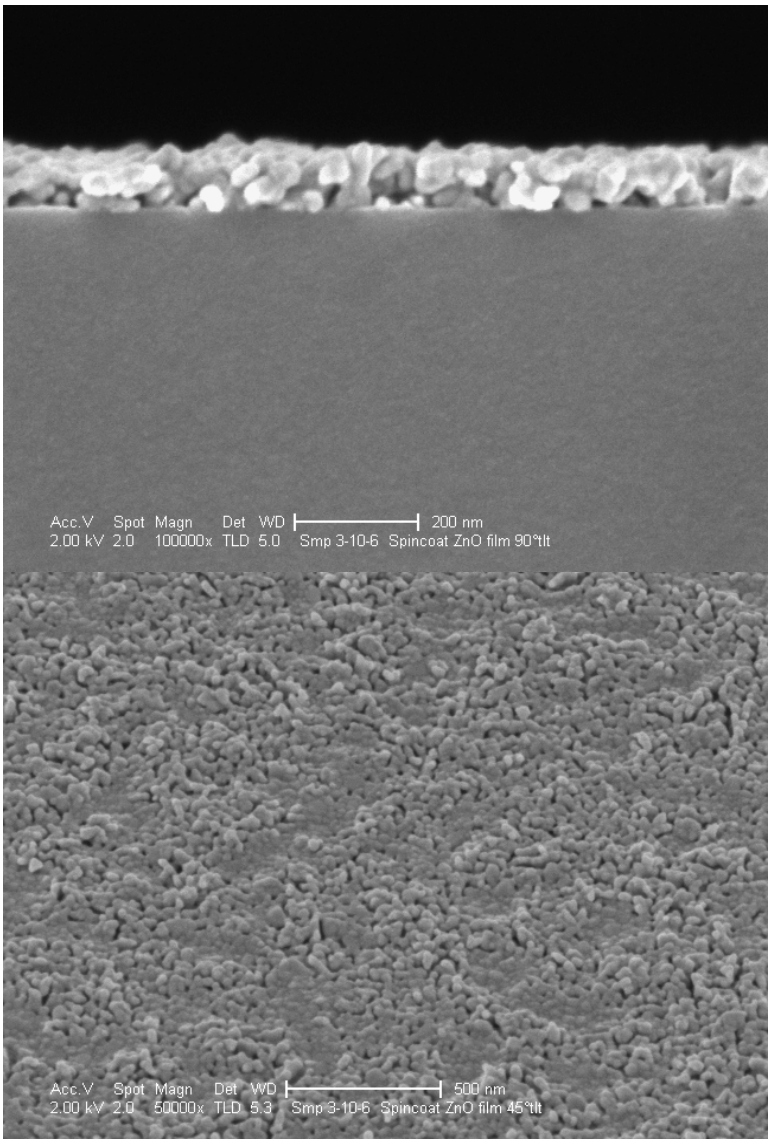

Figure 4.12: A side- and top-view SEM image with a 200 nm and 500 nm scale, respectively. These are images of a spin-coated ZnO film using a zinc nitrate spin solution pre-baked at $300°C$ in air on a Corning^{TM} 1737 glass substrate. [114] Notice that the grain size apparent in the top-view is $\sim 15 - 25$ nm.

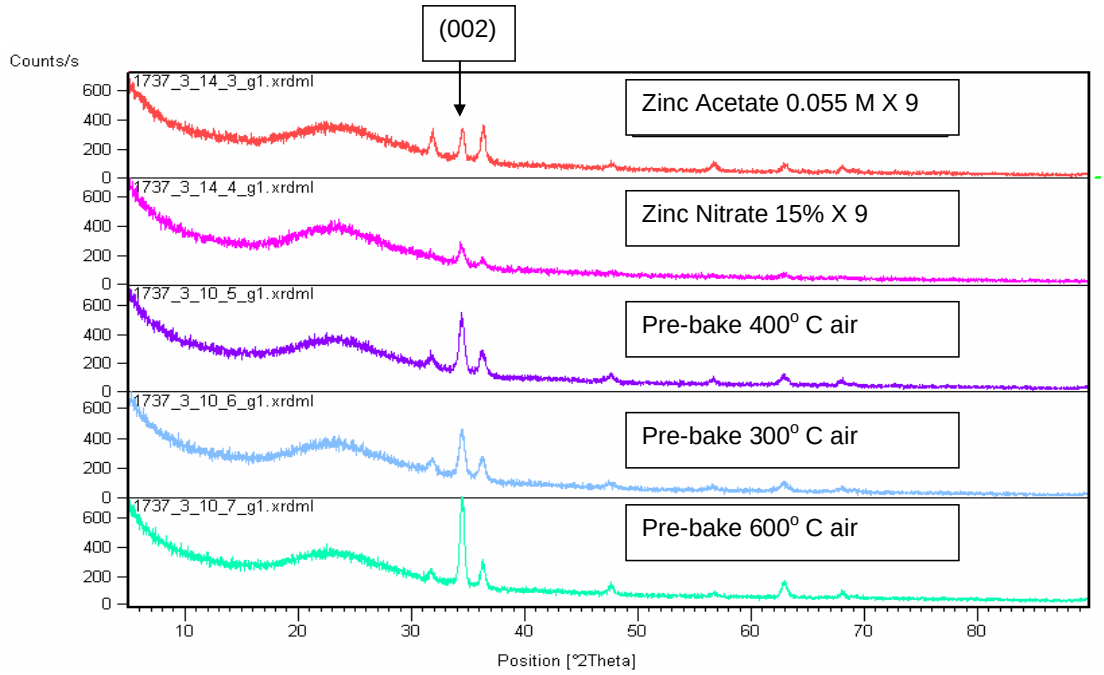

Figure 4.13: XRD patterns of spin-coated ZnO thin-films with different pre-bakes and which are deposited onto Corning^{TM} 1737 glass substrates. [114]

grain sizes of the two films are nearly identical at 17.5 and 16.9 nm for the 300°C pre-bake and the 600°C final bake films, respectively.

In the pre-bake experiment, the solvent bake step is omitted, with the operative hypothesis that the pre-bake should remove all of the solvent, so that the extra solvent bake is not necessary. This hypothesis appears to be correct since the 300°C pre-baked film is very similar to the 600°C RTAed film from the final bake experiment, as shown in Figs. 4.12 and 4.5.

Based on the pre-bake and final bake experiments, the best annealing conditions for the zinc nitrate-based spin solution used in this dissertation involve a 600°C pre-bake followed by a 600°C RTA in O_2. Unless otherwise noted, these annealing conditions are used for all of the ZnO thin-films discussed in the remainder of this dissertation.

4.2.1.4 Spin-Coated ZnO Thickness Versus thin-film Quality

Since zinc nitrate conversion to ZnO is a process that occurs from the film surface down, as evident from Fig. 4.8, it is reasonable to assume that the spin solution film thickness prior to thermal processing may strongly effect the ZnO film quality. Thus, an experiment involving five different solution viscosities is performed. The spin solutions are labelled by their percent concentration, where 100% indicates a solution made by the procedure given in Sec. 3.1.4.1. Percentages indicate the percent of 100% solution to deionized water, so that a 50% solution is 1 part deionized water to 1 part 100% solution. The solutions used for this investigation are 100%, 50%, 25%, 15%, and 10% zinc nitrate solutions.

Table 4.2 summarizes the results of the thickness study. Since AFM analysis is readily available at Oregon State University, while SEM assessment is not, this study is accomplished using AFM. However, SEM is often more desirable for this type of analysis, since it provides more details about the thin-film structure. Also, XRD analysis is not useful for this type of study since the signal becomes very weak as the films become thin. Included in Table 4.2 are RMS roughness, estimated substrate depth, and grain size, as discussed in Sec. 3.3.6, along with the spin solution used and the appropriate figure reference. Also, included in Table 4.2 is the profilometer thickness measured from a ZnO TTFT patterned using the same spin solution and processing recipe.

The AFM images of the thin-films made from the 100%, 50%, and 25% zinc nitrate solutions appear to be very similar, as shown in Figs. 4.14 and 4.15. Additionally, the RMS roughnesses are similar, as expected giving values of 6.1, 5.5, and 5.5 nm for the 100%, 50%, and 25% solutions, respectively. The estimated substrate depth does not vary significantly among these samples, indicating that the

Table 4.2: A summary of parameters of ZnO thin-films prepared using different types of spin solutions. §indicates a grain size obtained from XRD results.

Solution	SEM/AFM Fig.	XRD Fig.	RMS Roughness (nm)	Estimated Substrate Depth (nm)	AFM Grain Size (nm)	Profilometer Thickness (nm)
Zn Nit. 100%	4.14	-	6.1	24.7	18.7	75
Zn Nit. 50%	4.15	-	5.5	22.2	18.7	58
Zn Nit. 25%	4.16	-	5.5	29.7	13.1	32
Zn Nit. 15%	4.17	-	3.2	13.6	7.3	15
Zn Nit. 10%	4.18	-	2.8	10.1	7.3	~ 10
Zn Nit. 15% $\times$ 9	4.19	4.13	-	-	16.5 ± 2§	~ 10
Zn Acet. 0.3M	-	-	-	-	-	36
Zn Acet. 0.2M	-	-	-	-	-	14
Zn Acet. 0.055M$\times$9	4.20	4.13	-	-	22.1 ± 3§	~ 20

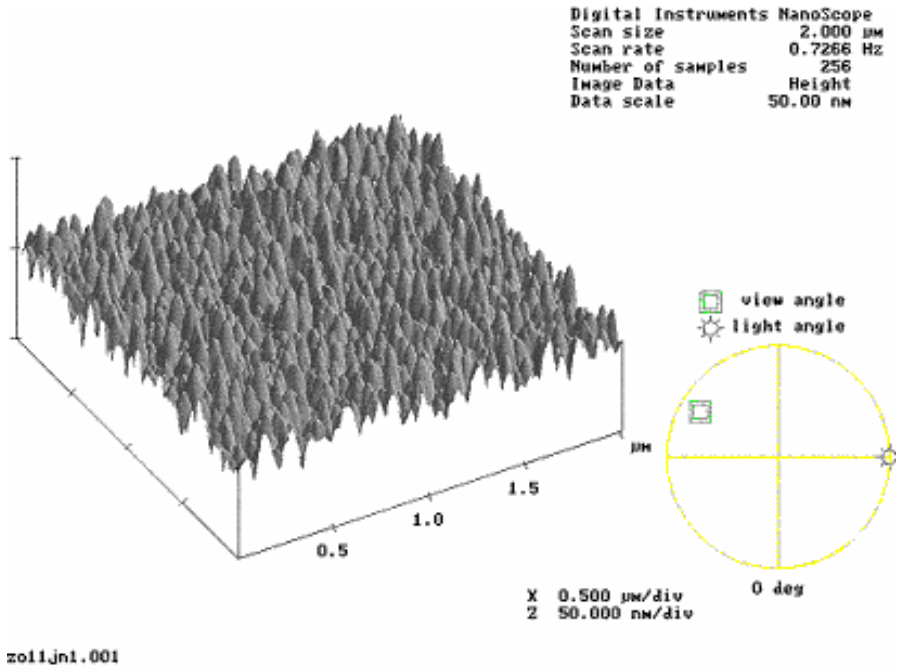

Figure 4.14: AFM image of a spin-coated ZnO thin-film on a Corning^{TM} 1737 glass substrate. This film is spun from a 100% concentration zinc nitrate spin solution. [114]

pore depth is likely to be ~ 25 nm. Measured AFM grain sizes of 18.7, 18.7, and 13.1 nm for the 100%, 50%, and 25% solutions, respectively, are in agreement with the calculated XRD grain size of 25 nm obtained for similar annealing conditions in the final bake analysis.

The AFM images of the thin-films synthesized from the 15% and 10% zinc nitrate solutions, as shown in Figs. 4.17 and 4.18, are noticeably smoother than the thin-films obtained using higher percentage spin solutions. This is confirmed by the the RMS roughnesses of 3.2 and 2.8 nm for the 15% and 10% zinc nitrate solutions, respectively, compared to ≥ 5.5 nm for films obtained using higher percentage solutions. Also, notice that the grain sizes and estimated substrate depths

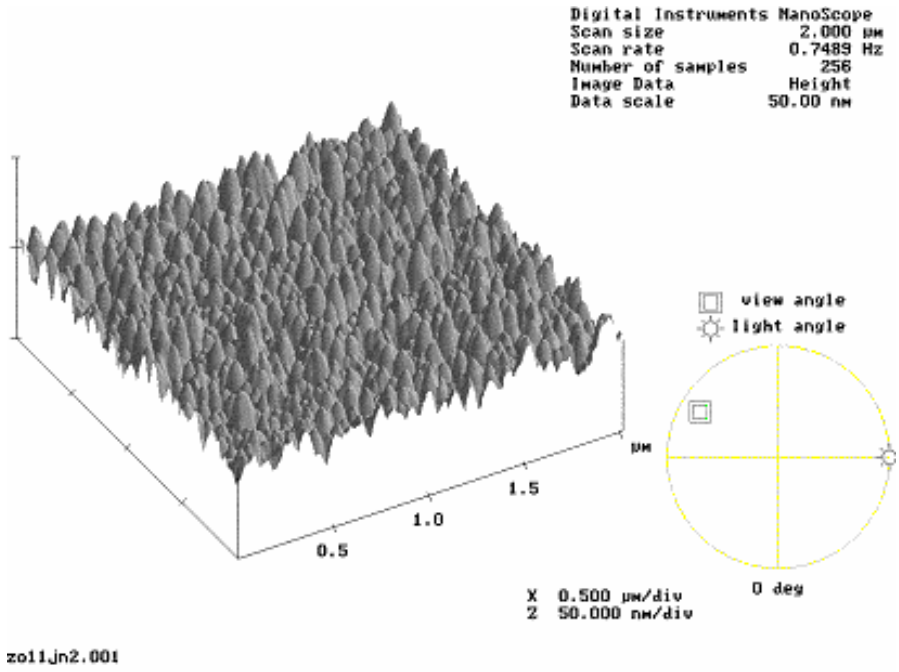

Figure 4.15: AFM image of a spin-coated ZnO thin-film on a Corning^{TM} 1737 glass substrate. This film is spun from a 50% concentration zinc nitrate spin solution. [114]

are approximately equal to the film thicknesses for the 15% and 10% zinc nitrate solutions.

The estimated substrate depth (29.7 nm) and film thickness (32 nm) are nearly equal for the 25% zinc nitrate solution. Additionally, the grain size is on the same order as the film thickness. Thus, thin-films from the 25% zinc nitrate solution solution are approximately one grain thick. Films $\sim$ 30 nm should produce the fewest grain boundaries and thus the highest quality films for ZnO TTFT applications, as discussed in Sec. 5.2.1. Films thicker than $\sim$ 30 nm will produce films that are multiple grain layers thick, so that the bottom layer may not nucleate in alignment with the substrate since the growth occurs from the film surface down, as shown in Fig. 4.8. Additionally, films thinner than $\sim$ 30 nm will limit grain growth sim-

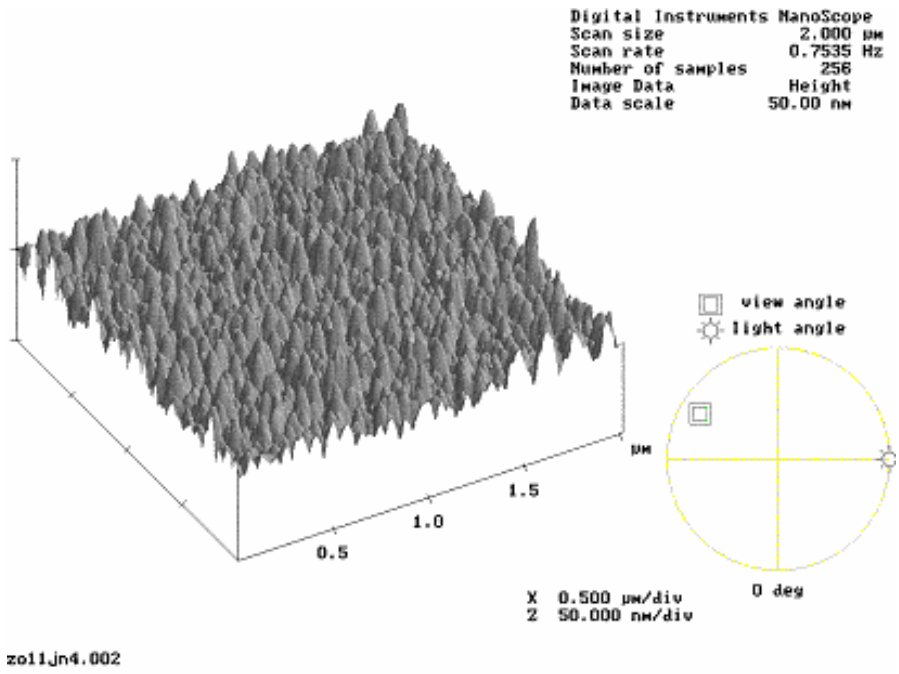

Figure 4.16: AFM image of a spin-coated ZnO thin-film on a Corning^{TM} 1737 glass substrate. This film is spun from a 25% concentration zinc nitrate spin solution.

ply due to the thickness of the film since the grains cannot be larger than the film thickness.

4.2.2 Multiple Layer Spin-Coating

Since the optimal thickness for converting zinc nitrate to ZnO is rather thin ($\sim 30\ nm$) it seems reasonable that spinning multiple layers onto a substrate could produce a high quality thin-film of greater thickness. To explore this, a 15% concentration zinc nitrate spin solution is spin-coated onto a Corning^{TM} 1737 substrate nine times. After each spin the substrate is baked on a hot plate for 10 min at $115°C$ and then placed in a furnace at $600°C$ for 10 min. Unfortunately, the layers did not build upon each other, so that the final thin-film is only slightly thicker

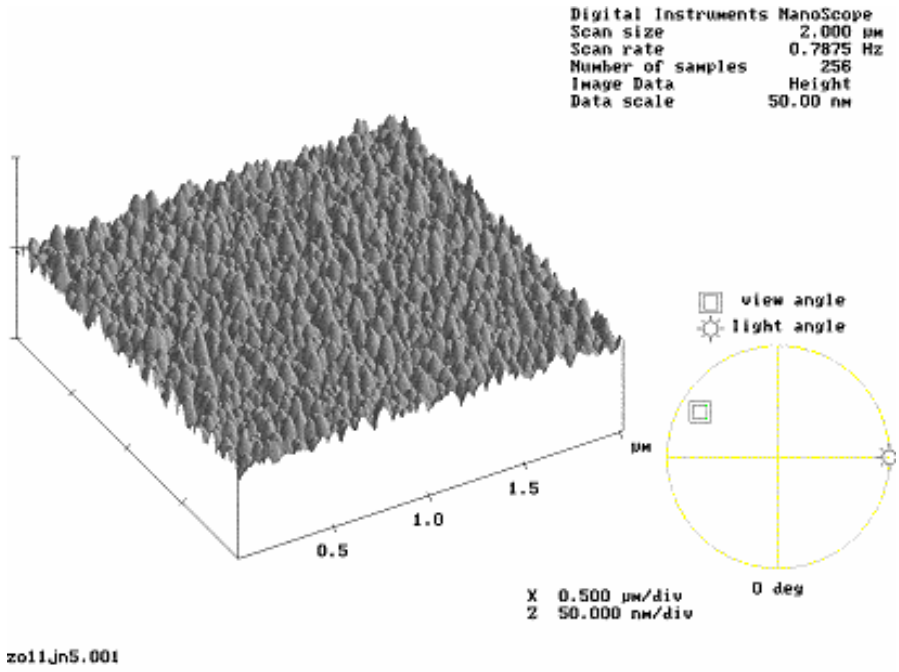

Figure 4.17: AFM image of a spin-coated ZnO thin-film on a Corning^{TM} 1737 glass substrate. This film is spun from a 15% concentration zinc nitrate spin solution. [114]

than that obtained from a single coat, as shown in Fig. 4.19 and Table 4.2. It is possible that the zinc nitrate spin solution is a mild ZnO etchant, so that each new layer etches the previously-deposited layer. Another possibility is that subsequent spin deposited layers are not able to stick to the previous ZnO layer. Both of these problems may be circumvented by spinning a thicker layer during each spin.

4.2.3 Zinc Acetate-Based Spin Solutions

As a means of comparing the spin-coating methods developed in this dissertation to a more standard method, films are prepared in a manner similar to that published for zinc acetate spin solutions. [62] A 0.055 M zinc acetate solution is

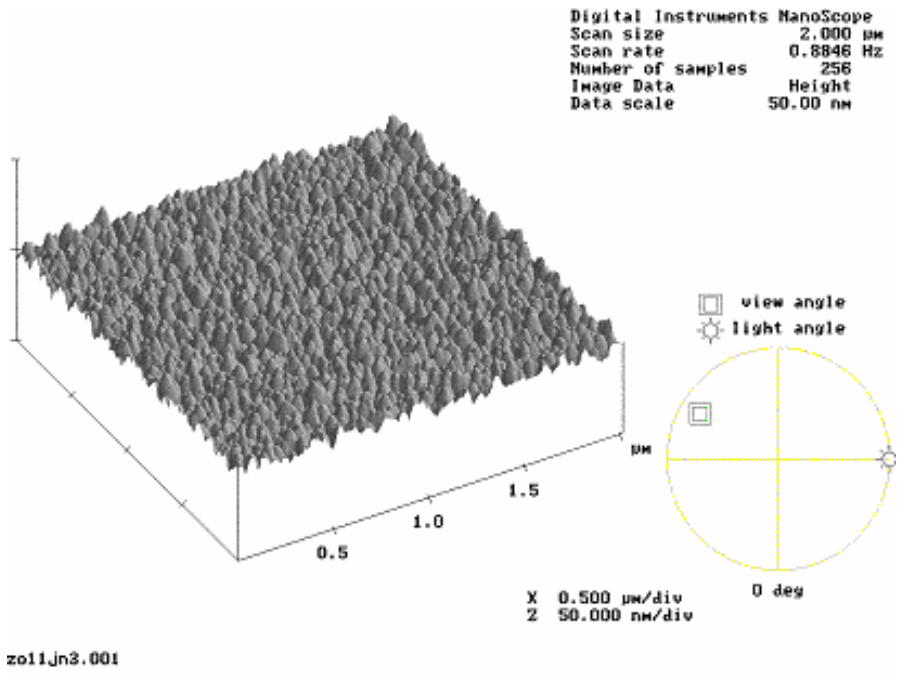

Figure 4.18: AFM image of a spin-coated ZnO thin-film on a Corning^{TM} 1737 glass substrate. This film is spun from a 10% concentration zinc nitrate spin solution. [114]

prepared and spin-coated onto a Corning^{TM} 1737 glass substrate at 3000 rpm for a total of nine repeat cycles. After each spin-coating deposition, the zinc acetate films are baked at 115°C on a hot plate for 10 min and then placed in an air oven for 10 min at 600°C. The thin-films produced from this method have an appearance similar to that of the 600°C pre-baked film, as shown in Figs. 4.20 and 4.10. In addition, the ZnO grain size is large, 22.1 nm, and comparable to the 600°C pre-bake result of 25 nm, as shown in Table 4.2. However, the XRD curve provides no evidence of preferred orientation, as shown in Fig. 4.13, as should be expected from the Natsume *et al.* result. [62] In addition, this film is much thinner than that obtained by Natsume *et al.*, $\sim$ 20 nm compared to 160 - 230 nm.

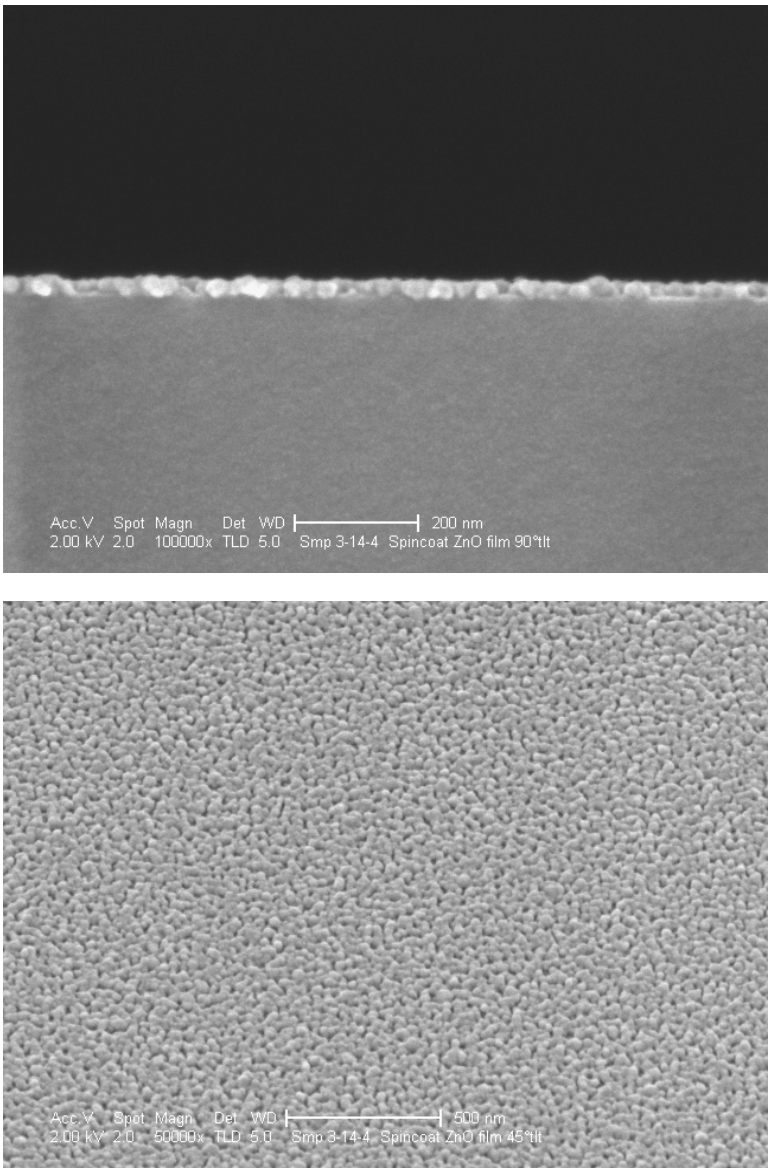

Figure 4.19: A side- and top-view SEM image with a 200 nm and 500 nm scale, respectively. These are images of a ZnO film on a Corning^{TM} 1737 glass substrate which is coated nine times with a 15% concentration zinc nitrate spin solution. [114]

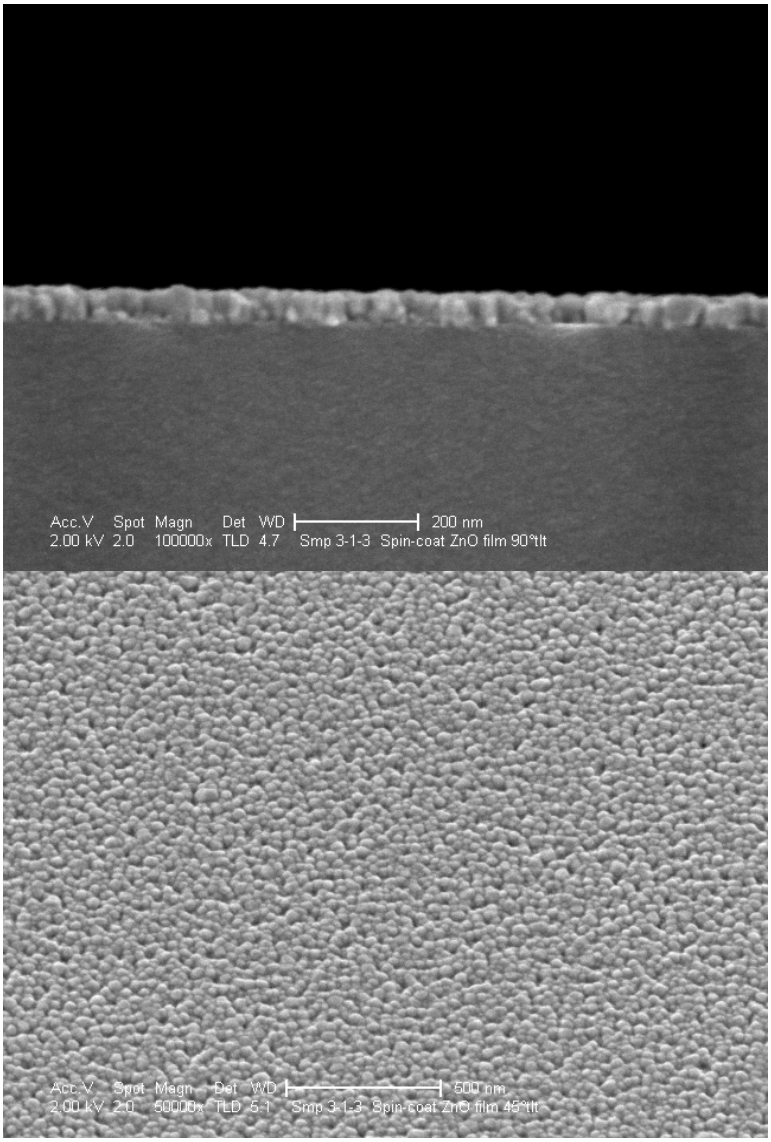

Figure 4.20: A side- and top-view SEM image with a 200 nm and 500 nm scale, respectively. These are images of a ZnO film on a Corning^{TM} 1737 glass substrate which is coated and annealed nine times with 0.055 M zinc acetate spin solution. [114]

Clearly something about solution phase deposition of zinc acetate is missing from the literature since the data presented here differs greatly from that reported by Natsume *et al.* However, this is not surprising since some research groups report well-oriented ZnO while others report random orientation for similar spin solutions and methods. [50, 52, 61] It is likely that these differences from one research group to the next are due to variations in annealing steps such as the temperature ramp or temperature gradient, since it is known from the work presented in this dissertation that these variables may strongly effect film quality. In addition, specific details about the annealing cycle are often left unpublished, *e.g.* temperature ramp, type of oven, placement within the oven, *etc.*

In order to compare a single coat of zinc acetate-based spin solution directly to that of a zinc nitrate solution, thin-films from 0.3 M and 0.2 M solution are prepared, as shown in Table 4.2. The resulting thin-films are thicker than those from the 0.055 M solution used for the multiple-coated film. The 0.3 M solution zinc acetate solution results in a ZnO thickness of 36 nm, which is similar to that of the 25% zinc nitrate solution at 32 nm. SEM and XRD data is not available for these acetate films, but the results of ZnO TTFTs constructed using these solutions are discussed in Sec. 5.2.2.

4.3 HfO_2 Spin-Coating

The insulating properties of HfO_2 suggest that it is a promising candidate as a TTFT gate insulator. This investigation explores HfO_2 deposition via spin-coating. Recent evidence suggests that HfO_2 gate TTFT mobility may be larger than that of SiO_2 gate ZnO TTFTs. [3, 4]

Table 4.3: A summary of HfO_2 film thickness and index of refraction(n) for various spin solutions.

Solution	Thickness (nm)	n
A	216.7	1.87
B	137.8	2.08
C (1 coat)	48.6	1.99
C (2 coats)	96.0	2.00
C (3 coats)	149.1	1.96
C (4 coats)	192.0	2.05

HfO_2 does not adhere well to ITO. Therefore, for the initial phase of this investigation, HfO_2 is spin-coated onto oxidized, heavily-doped Si wafers. The wafers are RTAed at $600°C$ in O_2 in order to oxidize just enough Si on the surface to produce a hydrophilic surface. Hf spin solutions are then spin-coated directly onto the Si wafer at 3000 rpm for 30 sec and then placed directly into a hot air furnace at $600°C$ for 5 min.

Table 4.3 summarizes the results of three HfO_2 spin solutions prepared by the recipe discussed in Sec. 3.1.4.3. The index of refraction (n) and the thickness are measured optically via diffuse reflectance. An index of refraction of 2 correlates well with that expected for HfO_2. [75, 117, 118, 119]. In addition, the multiple coats of solution C build up almost precisely at 50 nm per spin deposition. Solution A and B showed visible signs of cracking after the bake. However, the HfO_2 film from solution C is uniform and of high optical quality.

A $\sim 10\ nm$ adhesion layer of SiO_2 is deposited via PECVD onto an ITO-coated Corning^{TM} 1737 glass substrate to enable HfO_2 to be spin coated onto ITO. HfO_2 spin solution C is then spin coated onto the substrate four times and finally 0.08

cm^2 Al dots are evaporated on top. The loss tangent and dielectric constant versus frequency, shown in Fig. 4.21, are calculated from the capacitance and conductance versus frequency as measured by an HP model 4192A LF impedance analyzer. The current density versus electric field as measured by an HP model 4140B pA meter is shown in Fig. 4.22.

The relative dielectric constant of the metal insulator metal (MIM) stack is 11.5 at low frequency, as shown in Fig. 4.21. The capacitance of the stack is given by

$$C_{MIM} = \frac{\kappa \epsilon_0 A}{t_{MIM}}, \tag{4.1}$$

where κ is the relative dielectric constant, ϵ_0 is the permittivity of free space, A is the device area, and t_{MIM} is the MIM insulator thickness. Since the insulator of the MIM consists of HfO_2 and SiO_2 the MIM capacitance may be expressed as

$$1/C_{MIM} = 1/C_{SiO_2} + 1/C_{HfO_2}. \tag{4.2}$$

Thus,

$$t_{MIM}/\kappa_{MIM} = t_{SiO_2}/\kappa_{SiO_2} + t_{HfO_2}/\kappa_{HfO_2} \tag{4.3}$$

and the actual relative dielectric constant of the HfO_2 (κ_{HfO_2}), assuming that t_{SiO_2} is 5–15 nm and t_{MIM} is 205–215 nm , is 12.1–13.5. Typically, the dielectric constant of HfO_2 is ~ 25. [69, 70, 72] Additionally, the HfO_2 films spin coated onto ITO are not as transparent as expected, having a brownish color, as shown in Fig. 4.23. It is likely that the low dielectric constant and poor transparency are due to impurities in the chemicals used to make the HfO_2 spin solution. Further development will likely greatly improve the performance and transparency of spin-coated HfO_2.

HfO_2 spun onto ITO coated glass has a dielectric constant of 12.1–13.5, a loss tangent of 0.411%, a breakdown field of ~ 2.1 MV/cm, and a current leakage at 1 MV/cm of 17.37 nA/cm^2. Additionally, 200 nm and 400 nm thick HfO_2 have

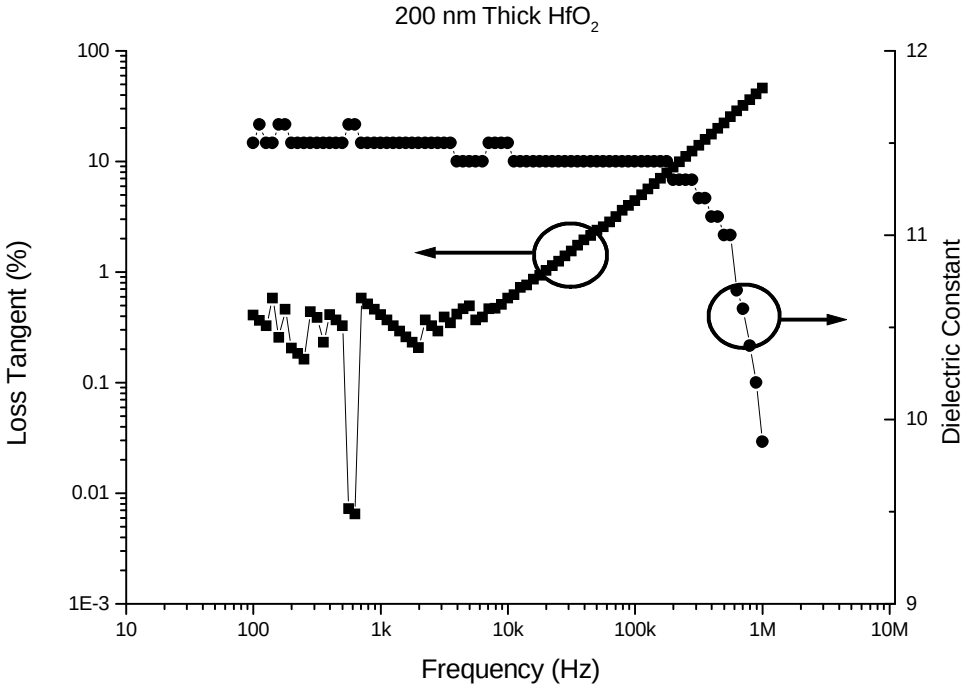

Figure 4.21: Dielectric constant and loss tangent versus frequency curves for an MIM capacitor stack consisting of a Corning^{TM} 1737 glass substrate coated with ITO, a $\sim 10\ nm$ PECVD layer of SiO_2, a 200 nm thick HfO_2 layer, and evaporated Al as a top contact. The dielectric constant and the loss tangent at 1 kHz are 11.5 and 0.411%, respectively.

similar dielectric constants, loss tangents, and dielectric breakdown fields indicating that the spin-coated HfO_2 is pinhole-free. The electrical performance of the spin-coated HfO_2 discussed in this dissertation is adequate for TTFT applications, as discussed in Sec. 5.3.

4.4 Conclusions

A crude SrS:Eu ACTFEL device in which the SrS:Eu phosphor layer is spin-coated is demonstrated. Additionally, spin-coated MgS shows promise as a method

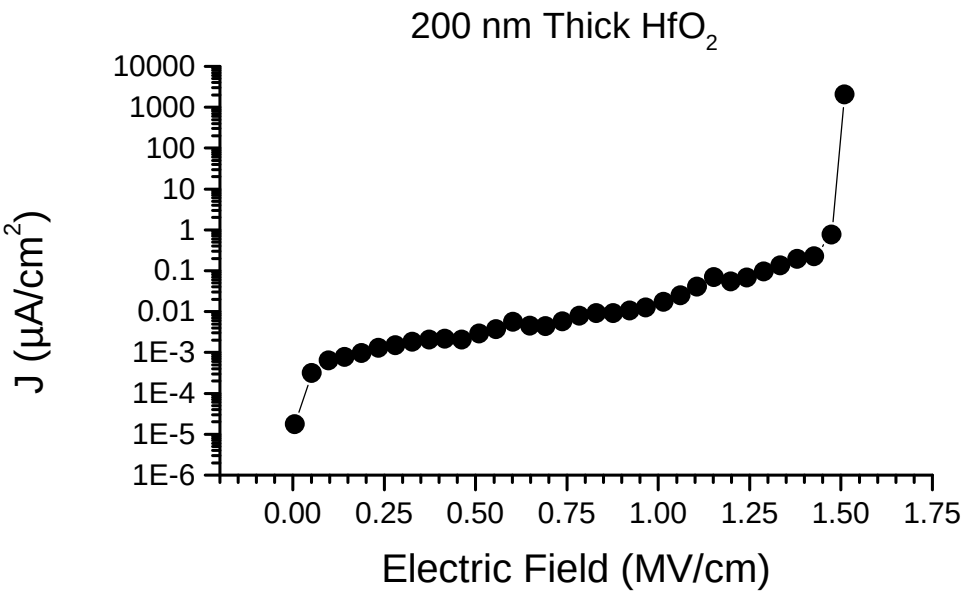

Figure 4.22: An electric field versus current density curve for an MIM capacitor consisting of a Corning^{TM} 1737 glass substrate coated with ITO, a $\sim 10\ nm$ PECVD layer of SiO_2, a 200 nm thick spin-coated HfO_2 layer, and evaporated Al as a top contact. The breakdown field is $\sim 2.1\ MV/cm$ and the current leakage at 1 MV/cm is 17.37 nA/cm^2.

of developing MgS. It is difficult produce MgS using traditional vacuum deposition methods. Thus, spin-coating MgS warrants further study.

Lessons learned from spin-coating deposition of phosphors are directly applicable to spin-coating deposition of other materials, *e.g* ZnO and HfO_2. Substrate cleaning is essential in spin-coating solution development since spin solutions do not adhere to improperly prepared substrates. Spin solutions should be filtered prior to spin-coating to minimize the possibility of particle contamination. The solvent should be tailored to the needs of a particular source material. Ethanol, methanol, and deionized water are generally good candidate solvents for a new spin solution. Adding glycine is often effective at preventing crystallization and increasing the solution viscosity. In addition, boiling glycine-based spin solutions results in a gel.

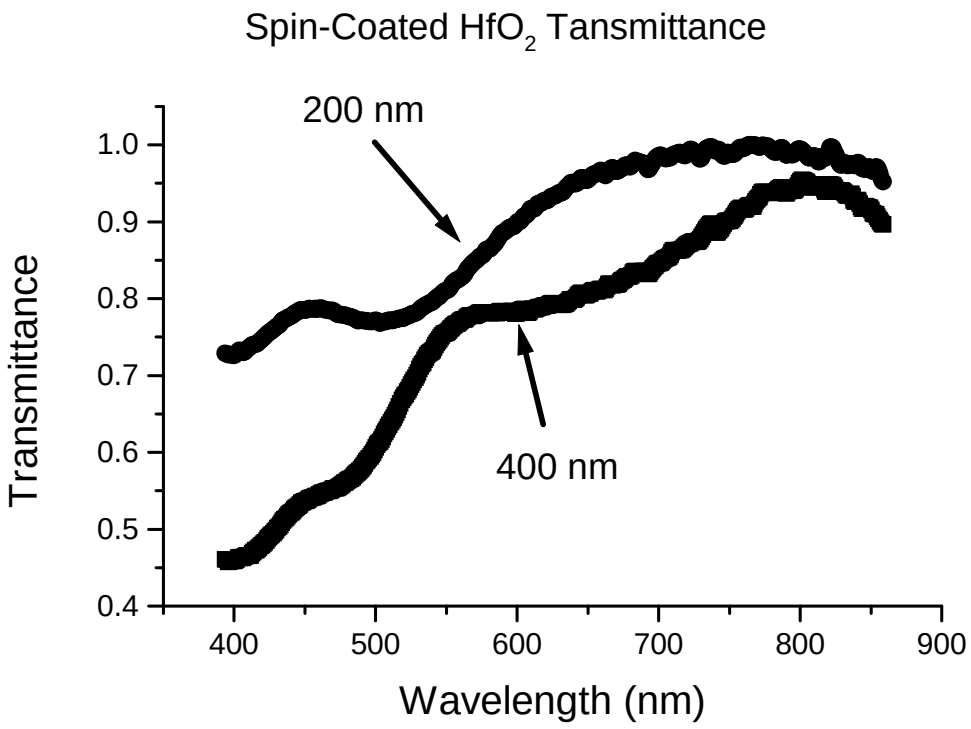

Figure 4.23: Transmittance versus wavelength curves for spin-coated HfO_2 with thickness of 200 and 400 nm. The substrate absorbtion curve has been subtracted out of these curves.

The highest quality ZnO thin-films from zinc nitrate-based solutions are obtained using a $600°C$ pre-bake followed by a $600°C$ RTA in O_2. Also, the optimal thin-film thickness for converting zinc nitrate to ZnO is ~ 30 nm.

HfO_2 spun onto ITO-coated glass has a dielectric constant of 12.1–13.5, a loss tangent of 0.411%, a breakdown field of ~ 2.1 MV/cm, and a current leakage at 1 MV/cm of 17.37 nA/cm^2. The HfO_2 dielectric constant is comparable to that of ATO, and the loss tangent and breakdown field are adequate for TTFT applications.

5. TTFT PROCESSING AND CHARACTERIZATION

In this chapter a photolithography process for ZnO TTFTs is qualified and then applied to spin-coated ZnO body and spin-coated HfO_2 gate insulator TTFTs. Additionally, this chapter contains ZnO TTFT electrical characteristics for top gate TTFTs and SiO_2 capped TTFTs.

Unless otherwise noted the results presented in this chapter are for bottom-gate, source and drain on top TTFTs prepared using NEG/ITO/ATO substrates. [99] The ZnO bodies are defined by photolithography with a mask, as shown in Fig. 3.6, and etched using an HCl wet etch. The ITO sources and drains are also defined photolithographically using a mask, as shown in Fig. 3.6, and patterned via lift-off. Devices with width-to-length ratios of 8 and 2 are tested and found to be consistent with each other. Thus, only data for TTFTs with a width-to-length ratio of 8 are shown in this chapter.

5.1 Ion-Beam Sputtered TTFTs

Ion-beam sputtering is used to deposit the ZnO for the TTFTs reported by Hoffman *et al.*. [1] Thus, ion-beam sputtered ZnO TTFTs are a good choice for comparison to spin-coated ZnO TTFTs. In addition, since the process for shadow masked TTFTs is well established for ion-beam sputtered ZnO TTFTs, it is useful to qualify a TTFT photolithography process using ion-beam sputtered ZnO TTFTs. [2]

Three ion-beam sputtered ZnO body thicknesses are tested in order to assess how body thickness effects TTFT operation. Since the film quality and crystal orientation are not likely to be strongly thickness dependent with ion-beam sputtered

ZnO, a thickness study is expected to unambiguously establish how electrical properties of the TTFT are effected by ZnO film thickness. Film quality is intimately related to film thickness for spin-coated ZnO, as discussed in Sec. 4.2.1.4; thus, it is more difficult to correlate TTFT electrical properties with ZnO body thickness using spin-coated ZnO TTFTs.

All of the data for the ion-beam sputtered TTFTs presented for the following thickness experiment are processed along side of each other, so that the source and drain ITO is the same. The ZnO body layers are RTAed after ZnO ion-beam sputter deposition at $700°C$ in oxygen.

5.1.1 Ion-beam Sputtered TTFT with a 78 nm Thick Body Layer

The $I_D - V_{DS}$ curves for the 78 nm body TTFT, as shown in Fig. 5.1, indicate a properly operating TTFT, similar to the shadow masked TTFT presented by Hoffman *et al.* [2, 1] The threshold voltage is found to be -3 V as calculated by a linear region $I_D - V_{GS}$ and saturation region $I_D^{1/2} - V_{GS}$ linear extrapolation to $I_D = 0$, as shown in Fig. 5.2 and discussed in Sec. 3.3.1. This TTFT saturates to a constant I_D for $V_{DS} \gg (V_{GS} - V_T)$, as shown in Fig. 5.1.

The mobility results of this TTFT are also in good agreement with the results of Hoffman *et al.*, as shown in Fig. 5.3. [2] μ_{eff} and μ_{FE} have a peak mobility of 0.49 and 0.51 cm^2/Vs, respectively. However, the curve for μ_{sat} has a peak value of 1.1 cm^2/Vs and deviates from the curves of μ_{eff} and μ_{FE}. This is not surprising since since μ_{sat} is calculated from $I_D - V_{GS}$ data with $V_{DS} = V_{GS}$ and this TTFT is not in saturation at $V_{DS} = V_{GS}$. V_T is positive for most TTFTs, so that when $V_{DS} = V_{GS}$ the TTFT operates in the saturation region; however V_T is negative for this device so that the condition $V_{DS} > (V_{GS} - V_T)$ is not met at $V_{DS} = V_{GS}$ for this

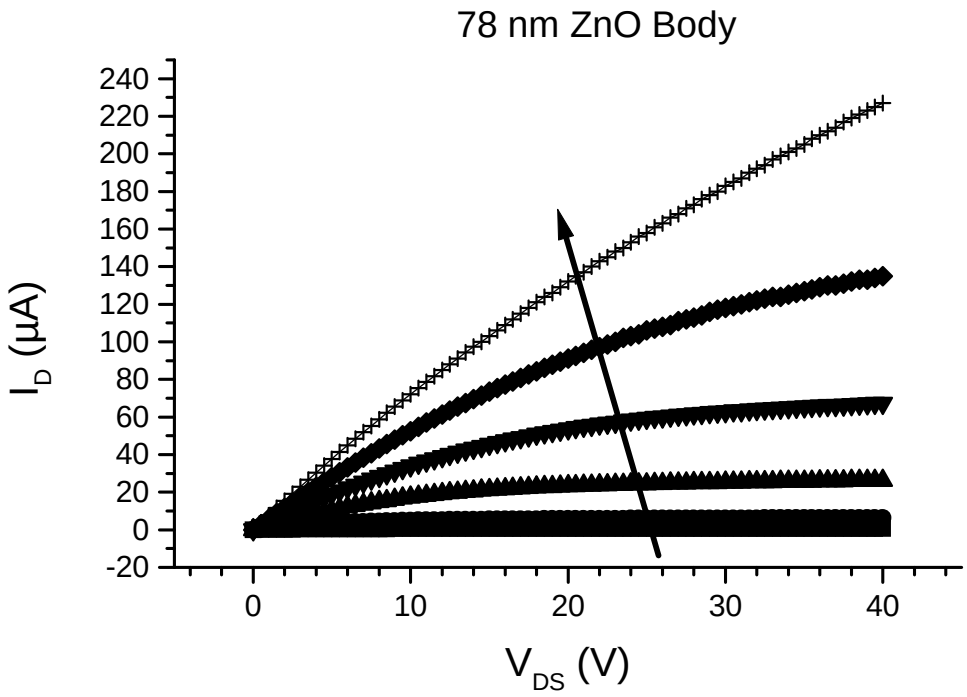

Figure 5.1: $I_D - V_{DS}$ curves for an ion-beam sputtered ZnO TTFT on a NEG/ITO/ATO substrate with a body thickness of 78 nm. Curves are shown for V_{GS} increasing from -10 to 40 V in 10 V increments, as indicated by an arrow. Notice that the $I_D - V_{DS}$ curves at $V_{GS} = 30$ and 40 V do not saturate since V_{DS} is not much greater than $(V_{GS} - V_T)$.

TTFT. Thus, μ_{sat} is not calculated in the saturation region, as it should be, and thus the estimated mobility is not accurate.

The 78 nm thick body TTFT defined by photolithography possesses similar characteristics to ZnO TTFTs defined by shadow masking, since shadow masked TTFTs have V_T's of 10–15 V and mobilities of 0.35–0.45 cm^2/Vs. [2] Thus, it may be concluded that TTFTs with lithography defined TTFT (300×400 μm) perform in a similar way to that of shadow masked TTFTs (4500×15000 μm). [2] Additionally, the TTFT performance is not greatly altered by the additional processing required for the photolithography process developed in this dissertation.

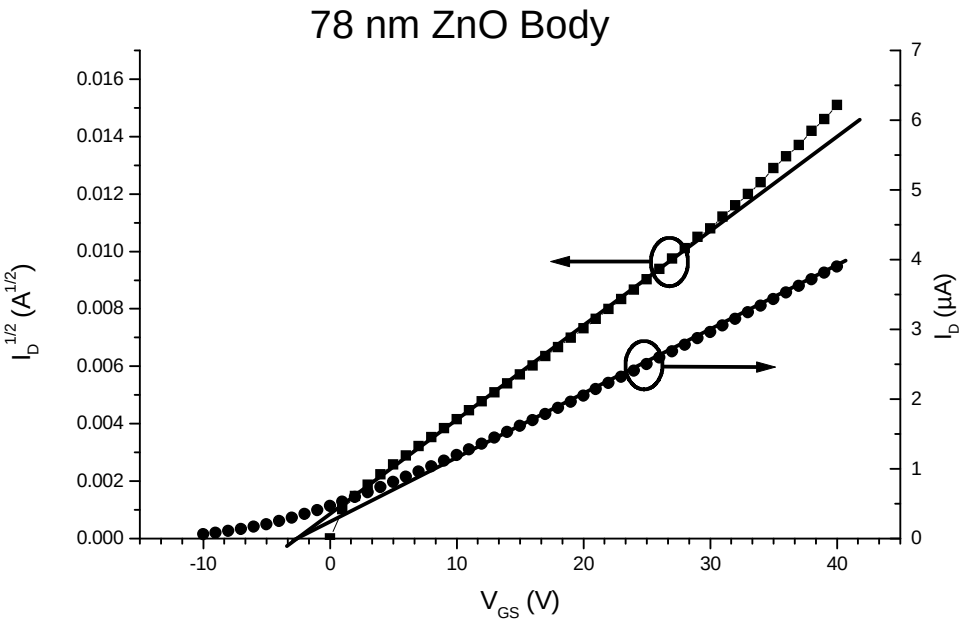

Figure 5.2: Linear region $I_D - V_{GS}$, $V_{DS} = 0.5\ V$, and saturation region $I_D^{1/2} - V_{GS}$, $V_{DS} = V_{GS}$, curves for an ion-beam sputtered ZnO TTFT with a body thickness of 78 nm on a NEG/ITO/ATO substrate. A linear extrapolation to $I_D = 0$ indicates a V_T of -3 V.

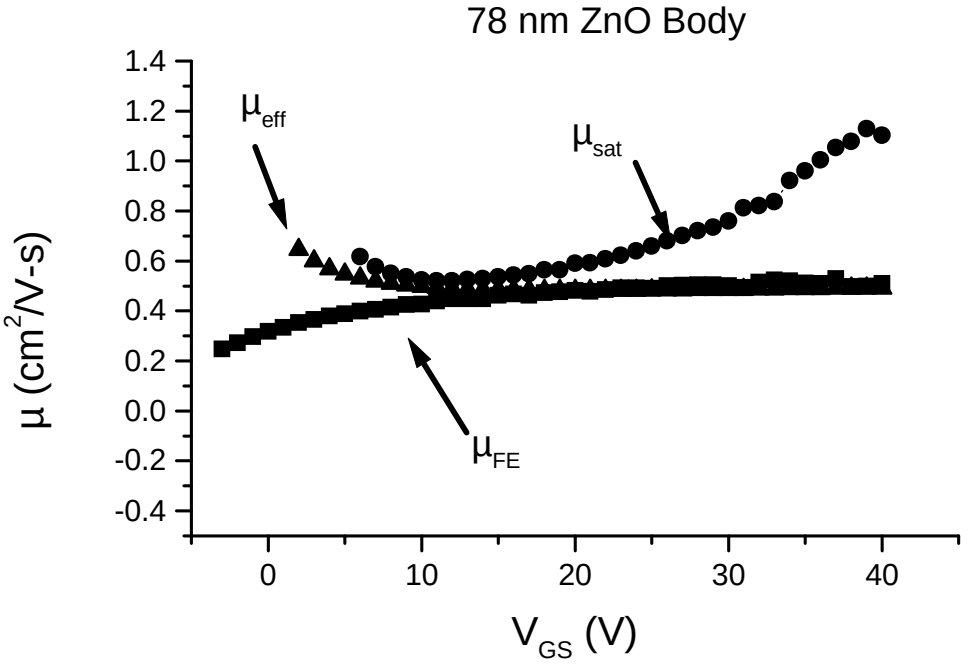

Figure 5.3: μ_{sat}, μ_{eff}, and μ_{FE} versus V_{GS} curves for an ion-beam sputtered ZnO TTFT with a body thickness of 78 nm on a NEG/ITO/ATO substrate.

5.1.2 Ion-beam Sputtered TTFT with a 333 nm Thick Body Layer

The $I_D - V_{DS}$ curves for the 333 nm thick body layer TTFT, as shown in Fig. 5.4, do not saturate to a constant I_D and have a large leakage current, indicating a small source to drain bulk resistance (R_B). R_B for a TFT due to the body layer bulk conductivity is

$$R_B = \frac{L\rho}{Wt}, \tag{5.1}$$

where t is the film thickness and ρ is the resistivity of the body layer. Notice that ρ/t is the sheet resistance of the body layer. Thus, R_B decreases as t is increases. From Fig. 5.4 the slope of the saturation portion of the $I_D - V_{DS}$ curves are between 0.06–0.6 $\mu A/V$, resulting in R_B = 16.7–1.67 $M\Omega$ and $\rho = 4.45 \times 10^2$–4.45×10^3 Ωcm from Eq. 5.1. These resistivity values are in the range of expected values for undoped ZnO.

V_T is calculated to be 12 V by the linear $I_D - V_{GS}$ method and 6 V by the $I_D^{1/2} - V_{GS}$ method, as shown in Fig. 5.5. A non-infinite R_B adds a term V_{DS}/R_B to the linear and saturation region equations, as shown in Eqs. 3.1 and 3.2, respectively, due to the fact that the measured I_D is comprised of both the channel current and the non-ideal leakage current associated with conduction in the 'bulk' body layer. Thus, when R_B is non-infinite a linear extrapolation of $I_D^{1/2} - V_{GS}$ and $I_D - V_{GS}$ does not result in $V_{GS} = V_T$ at $I_D = 0$.

μ_{eff}, μ_{FE}, and μ_{sat} peak values for this TTFT closely agree with each other at ~ 0.2 cm^2/Vs, as shown in Fig. 5.6. However, the mobility is smaller than the mobility calculated for the TTFT with the 78 nm thick body layer. This could be due, in part, to substrate-to-substrate TTFT variations and may not be related to changes in body thickness. However, a large, statistically significant data set

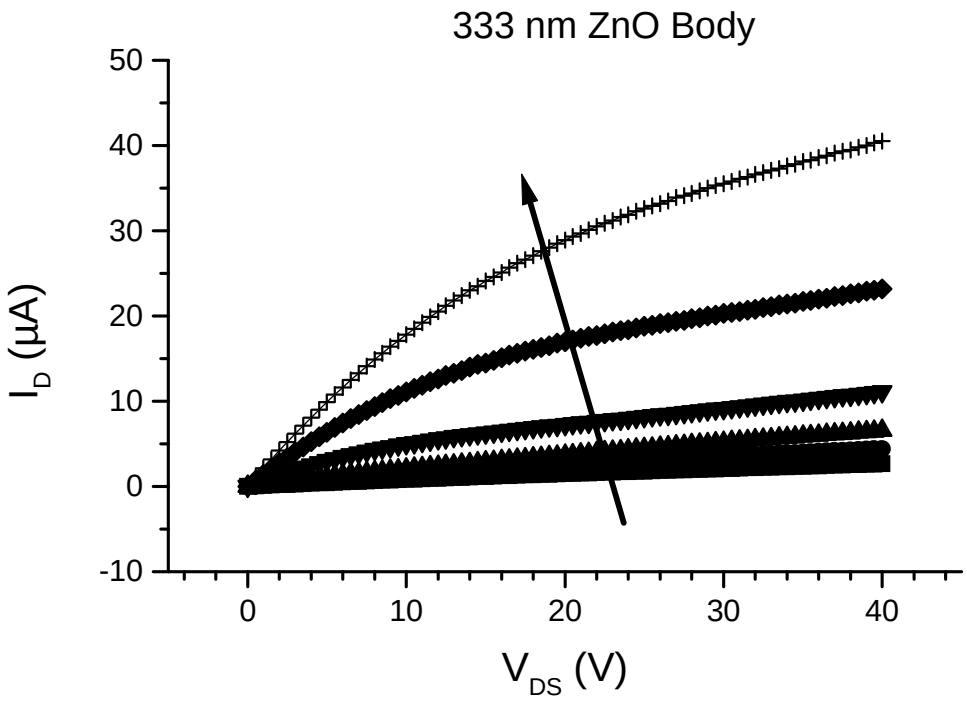

Figure 5.4: $I_D - V_{DS}$ curves for an ion-beam sputtered ZnO TTFT with a body thickness of 333 nm on a NEG/ITO/ATO substrate. Curves are shown for V_{GS} increasing from -10 to 40 V in 10 V increments, as indicated by an arrow.

would be required to conclusively relate device physics changes in mobility to process variations; such a project is not warranted at this early stage of technology development.

5.1.3 Ion-beam Sputtered TTFT with a 20 nm Thick Body Layer

The $I_D - V_{DS}$ curves for the 20 nm body TTFT, as shown in Fig. 5.7, saturate to a constant I_{DS} for $V_{GS} \leq 20\ V$; for $V_{GS} > 20\ V$ TTFT is not operating in the saturation region since V_{DS} is not much greater than $(V_{GS} - V_T)$. Constant I_{DS} in the saturation region of operation indicates that the source to drain bulk resistance

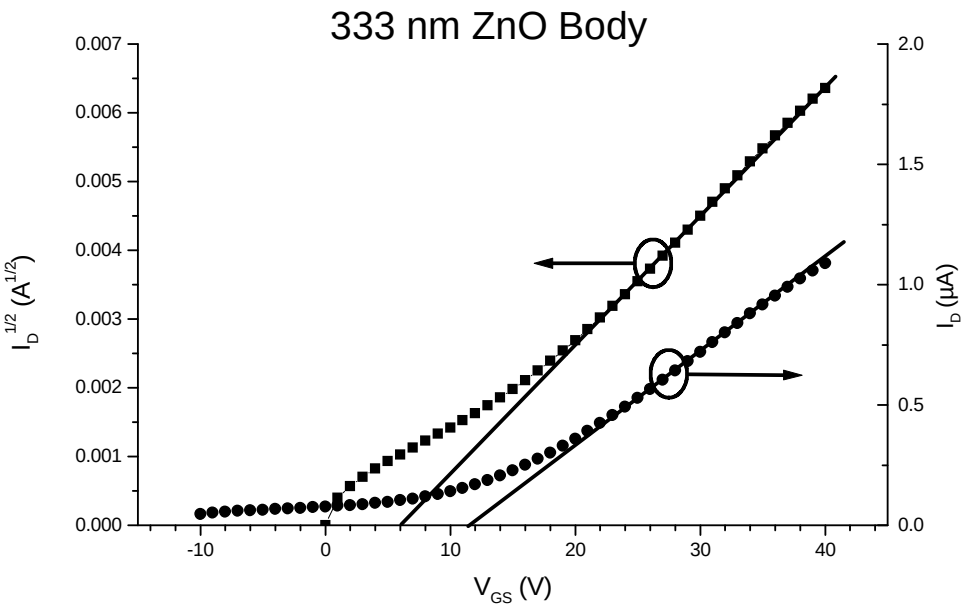

Figure 5.5: Linear region $I_D - V_{GS}$, $V_{DS} = 0.5V$, and saturation region $I_D^{1/2} - V_{GS}$, $V_{DS} = V_{GS}$, curves for an ion-beam sputtered ZnO TTFT with a body thickness of 333 nm on a NEG/ITO/ATO substrate. A linear extrapolation to $I_D = 0$ indicates a V_T of 6–12 V.

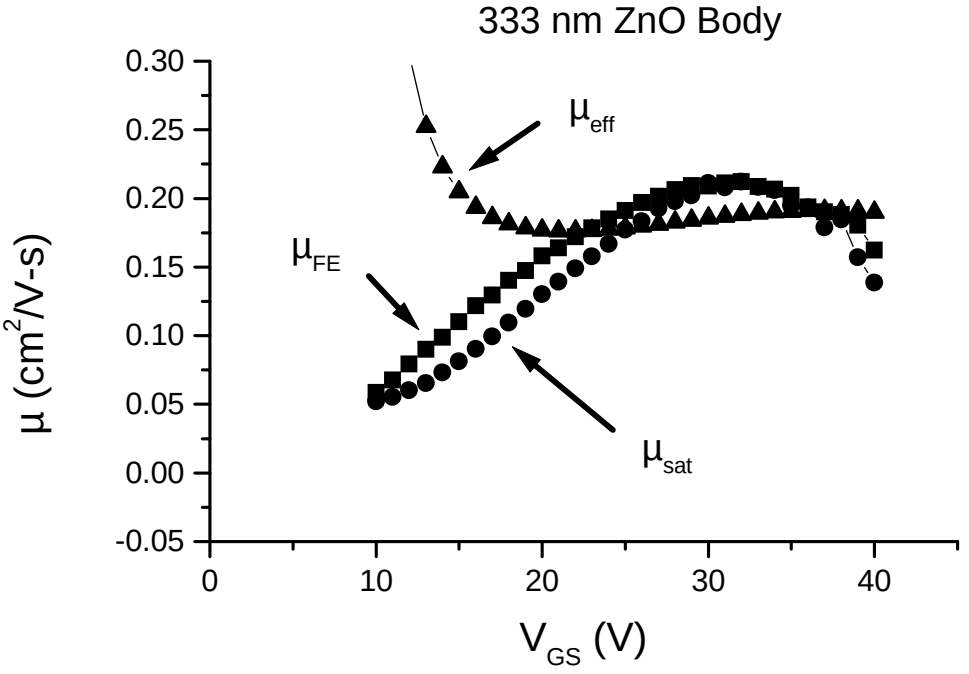

Figure 5.6: μ_{sat}, μ_{eff}, and μ_{FE} versus V_{GS} curves for an ion-beam sputtered ZnO TTFT with a body thickness of 333 nm on a NEG/ITO/ATO substrate.

(R_B) is large . R_B is expected to be very large for this device since the body layer is very thin. Additionally, notice that the $I_D - V_{DS}$ curves become I_D current limited for $V_{GS} > 30\ V$, i.e. there is very little increase in I_D between $V_{GS} = 30$ and 40 V curves, indicating a large source resistance (R_S). I_D current limmiting occurs when R_S and I_D are large enough that negative feedback is created at V_{GS}, as discussed in Sec. 3.3.1.

Source and drain resistance becomes a greater issue as transistor dimensions shrink since the current density at the source and drain become proportionally larger with smaller dimensions. For example the source and drain contact area of the Hoffman *et al.* TTFT with a width-to-length ratio of 10 is $2.25 \times 10^7\ \mu m^2$ whereas the source and drain contact area of the TTFTs constructed for this dissertation are $3.0 \times 10^4\ \mu m^2$. Thus, assuming that the current density is uniform across the source and drain, the current density at the source and drain of the TTFTs in this dissertation is 600 times larger than that of a Hoffman *et al.* TTFT at a similar bias condition. Additionally, as the body layer becomes very thin, the electric field near the edge of the source becomes larger, so that the current density is larger near the edge of the source. Thus, the current density demand on the source and drain contacts of thin-body TTFTs is even larger than expected by assuming a uniform current density across the source and drain, and $I_D - V_{DS}$ current crowding is exacerbated.

V_T for this 20 nm thick body layer TTFT is found to be 1 V, as calculated by the linear $I_D - V_{GS}$ method and 3 V as calculated by the $I_D^{1/2} - V_{GS}$ saturation method, as shown in Fig. 5.8. μ_{eff}, μ_{FE}, and μ_{sat} peak values closely agree with each other at a values of 0.82, 0.95, and 0.95 cm^2/Vs, respectively, as shown in Fig. 5.9. Mobility for this device is slightly larger than with the 78 and 333 nm body device, but is within the limits of observed substrate-to-substrate process variation.

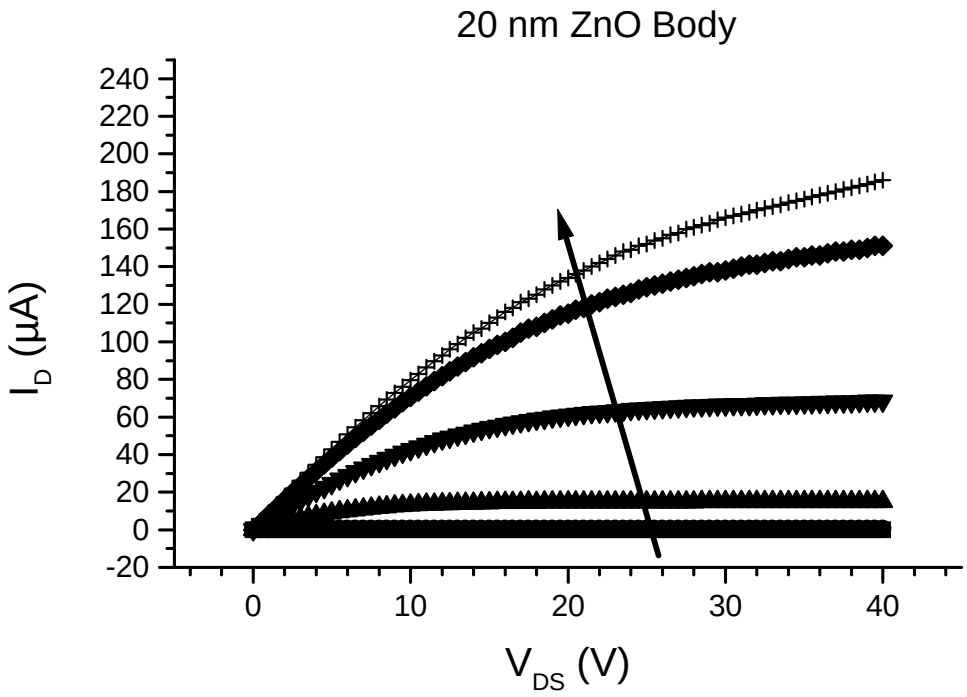

Figure 5.7: $I_D - V_{DS}$ curves for an ion-beam sputtered ZnO TTFT with a body thickness of 20 nm on a NEG/ITO/ATO substrate. Curves are shown for V_{GS} increasing from -10 to 40 V in 10 V increments, as indicated by an arrow. Notice that the $I_D - V_{DS}$ curves at $V_{GS} = 30$ and 40 V do not saturate since V_{DS} is not much greater than $(V_{GS} - V_T)$.

The I_D on-to-off behavior of ion-beam sputtered ZnO TTFTs with different body thicknesses is shown in Fig. 5.10. The on-to-off ratios are 8.6×10^5, 316, and 15 for the 20, 78, and 333 nm thick ZnO bodies, respectively. Thus, the I_D on-to-off performance improves greatly as the body thickness is decreased. This is expected from Eq. 5.1, since R_B increases as the body thickness decreases.

5.1.4 Conclusions

Photolithography is demonstrated to be a viable method for producing TTFTs with small device dimensions, yielding device performance similar to that obtained

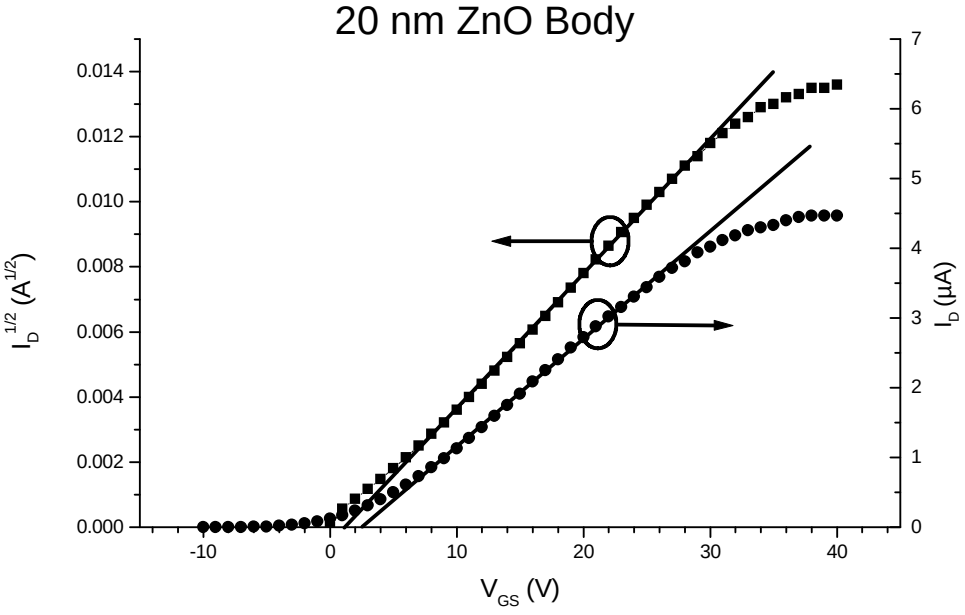

Figure 5.8: Linear region $I_D - V_{GS}$, $V_{DS} = 0.5V$, and saturation region $I_D^{1/2} - V_{GS}$, $V_{DS} = V_{GS}$, curves for an ion-beam sputtered ZnO TTFT with a body thickness of 20 nm on a NEG/ITO/ATO substrate. A linear extrapolation to $I_D = 0$ indicates a V_T of 1–3 V.

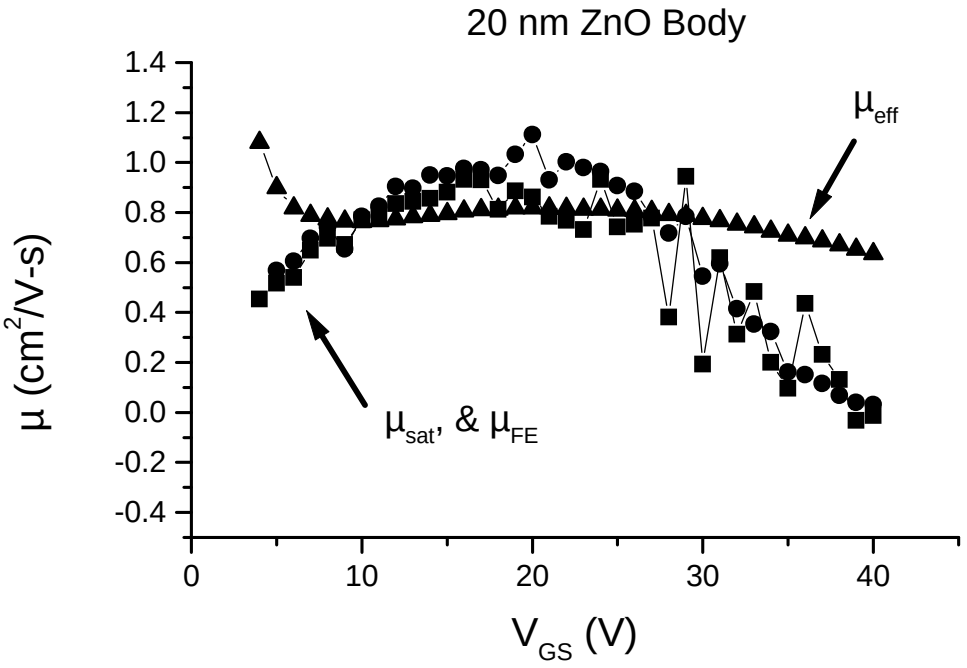

Figure 5.9: μ_{sat}, μ_{eff}, and μ_{FE} versus V_{GS} curves for an ion-beam sputtered ZnO TTFT with a body thickness of 20 nm on a NEG/ITO/ATO substrate.

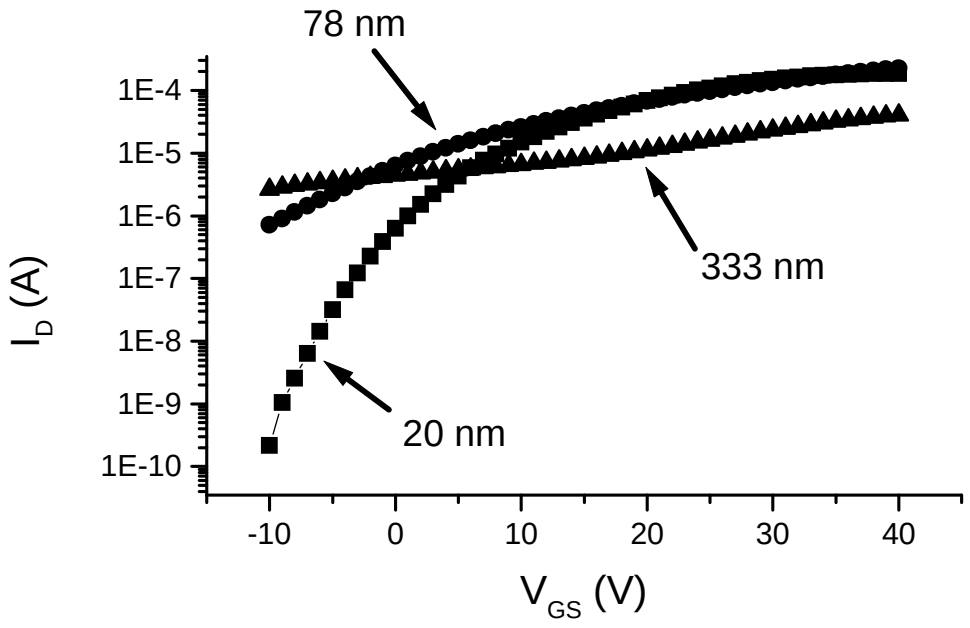

Figure 5.10: Semi-log $I_D - V_{GS}$ curves for a ion-beam sputtered ZnO TTFT with body thicknesses of 20, 78, and 33 *nm* on NEG/ITO/ATO substrates.

for shadow masked TTFTs. However, performance tradeoffs do exist. $I_D - V_{DS}$ current crowding becomes problematic as device dimensions and body thickness are decreased. In addition, R_B decreases as the body thickness is increases resulting in a poor I_D on-to-off performance.

5.2 Spin-Coated TTFTs

5.2.1 Spin-Coated TTFT Body Thickness

Spin-coated ZnO thin-film quality strongly depends on the thickness of the thin-film, as discussed in Sec. 4.2.1.4. Thus, the performance of ZnO TTFTs with spin-coated ZnO body layers is depends greatly on the body thickness. It is helpful to keep in mind the results of the ion-beam sputtered body thickness study when

assessing spin-coated ZnO TTFTs, so that body thickness related behavior may be extracted from body quality related behavior.

Bottom gate, source and drain on top TTFTs on NEG/ITO/ATO are constructed with ZnO bodies prepared from 100%, 50%, 25%, 15%, and 10% zinc nitrate spin solutions. Each spin solution is coated using a 3000 rpm spin for 15 sec followed by a 500 rpm for 15 sec drying spin. Then the zinc nitrate films are converted to ZnO with a 10 min air oven bake at 600°C followed by a 700°C RTA in O_2. The remaining process steps are identical to the process steps for the ion-beam sputtered TTFTs, as discussed in Sec. 5.1. The resulting ZnO body thicknesses are measured to be 75, 58, 32, $\sim$ 15, and $\sim$ 10 nm for the 100%, 50%, 25%, 15%, and 10% zinc nitrate spin solutions, respectively.

The TTFT made from the 100% zinc nitrate spin solution, with a body thickness of 75 nm, exhibits poor saturation behavior, as shown Fig. 5.11, indicating a small R_B. The slope of the $I_D - V_{DS}$ curves in the saturation region indicates a R_B of 5–50 $M\Omega$ and ρ equal to 300–3000 Ωcm. Thus, ρ is only slightly smaller for this device compared to that of the ion-beam sputtered TTFTs. V_T, μ_{eff}, μ_{FE}, and μ_{sat} are calculated to be -20 V, $\sim$0.01, $\sim$0.02, and $\sim$0.02 cm^2/Vs, respectively. Small mobility suggests that the ZnO is defect-rich, as expected from AFM data, as discussed in Sec. 4.2.1.4.

Electrical performance is not greatly improved for a ZnO TTFT made from the 50% zinc nitrate spin solution, as shown in Fig. 5.12. Although the saturation behavior is much better, further electrical assessment indicates that the mobility is still very small. V_T, μ_{eff}, μ_{FE}, and μ_{sat} are calculated to be -4 V, $\sim$0.01, $\sim$0.01, and $\sim$0.014 cm^2/Vs, respectively.

The electrical performance of a spin-coated ZnO TTFT fabricated using a 25% zinc nitrate spin solution, and having a body thickness of 32 nm, as shown in

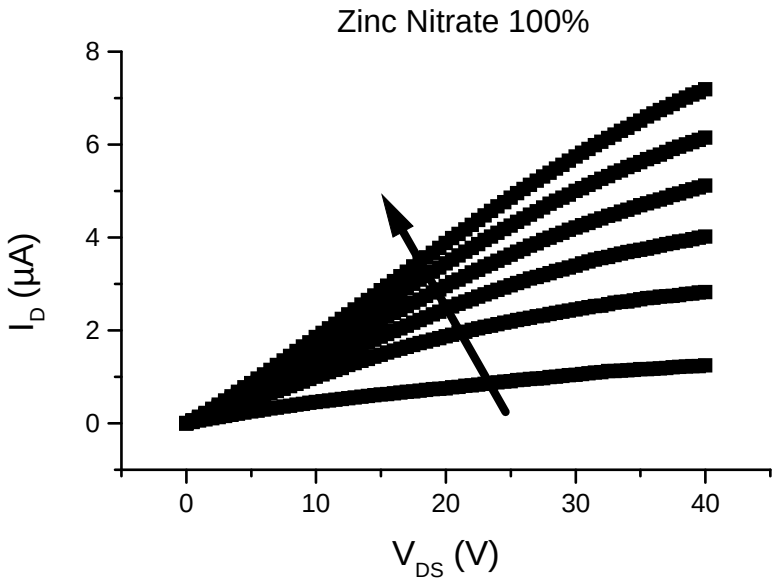

Figure 5.11: $I_D - V_{DS}$ curves for spin-coated ZnO TTFT fabricated using a 100% zinc nitrate spin solution with a thickness of 75 nm on a NEG/ITO/ATO substrate. Curves are shown for V_{GS} increasing from -10 to 40 V in 10 V increments as indicated by an arrow.

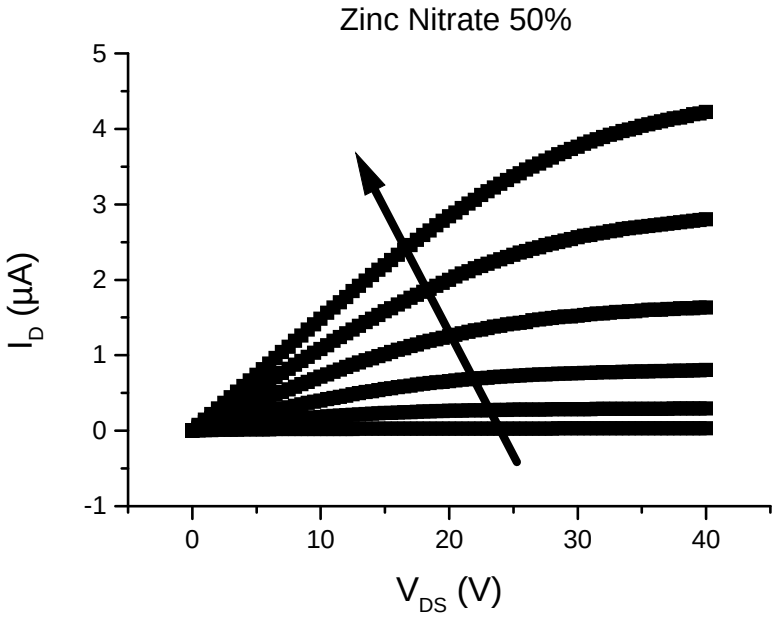

Figure 5.12: $I_D - V_{DS}$ curves for spin-coated ZnO TTFT fabricated using a 50% zinc nitrate spin solution with a body thickness of 58 nm on a NEG/ITO/ATO substrate. Curves are shown for V_{GS} increasing from -10 to 40 V in 10 V increments as indicated by an arrow.

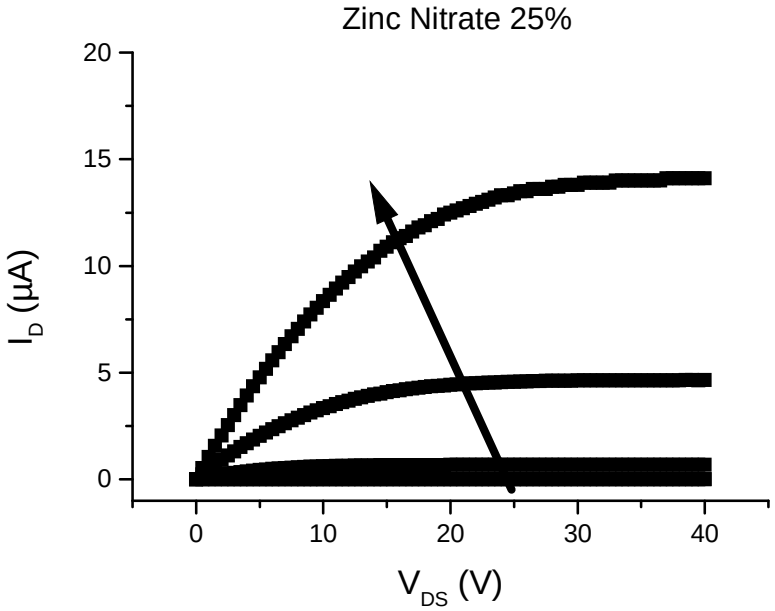

Figure 5.13: $I_D - V_{DS}$ curves for spin-coated ZnO TTFT fabricated using a 25% zinc nitrate spin solution with a body thickness of 32 nm on a NEG/ITO/ATO substrate. Curves are shown for V_{GS} increasing from 0 to 40 V in 10 V increments as indicated by an arrow.

Figs. 5.13, shows large improvement over the TTFTs made with thicker spin-coated bodies. The saturated I_D current is nearly constant, indicating a large R_B. V_T is calculated to be 22 V by the linear $I_D - I_{GS}$ method and 16 V by the $I_D^{1/2} - V_{GS}$ saturation method, as shown in Fig. 5.14. Mobility versus V_{GS} curves, as shown in Fig. 5.15, indicate peak μ_{eff}, μ_{FE}, and μ_{sat} of 0.14, 0.16, and 0.2 cm^2/Vs, respectively. The mobility is much larger compared to spin-coated ZnO TTFTs made with thicker spin-coated bodies and nearly as large as the mobilities obtained with ion-beam sputtered TTFTs.

A spin-coated ZnO TTFT fabricated using a 15% zinc nitrate solution, with a body thickness of ~ 15 nm, has poor electrical performance compared to that of the TTFT from the 25% zinc nitrate solution, which has a body thickness of 32 nm. The $I_D - V_{DS}$ curves, as shown in Figs. 5.16, do show transistor behavior, but I_D is

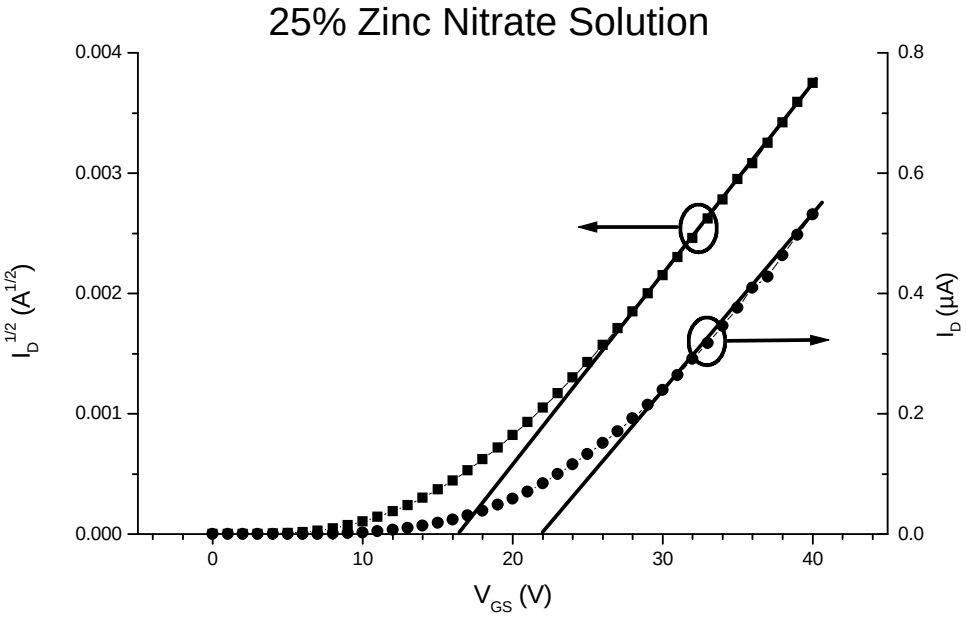

Figure 5.14: Linear region $I_D - V_{GS}$, $V_{DS} = 0.5\ V$, and saturation region $I_D^{1/2} - V_{GS}$, $V_{DS} = V_{GS}$, curves for a spin-coated ZnO TTFT fabricated using 25% zinc nitrate spin solution with a body thickness of 32 nm on a NEG/ITO/ATO substrate. A linear extrapolation to $I_D = 0$ indicates a V_T of 16 V.

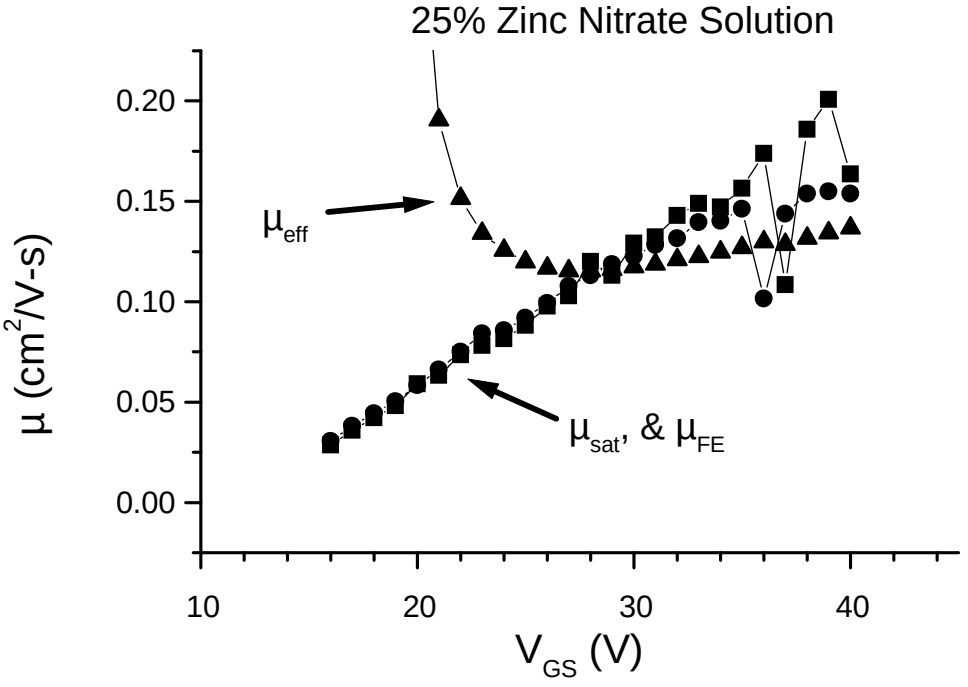

Figure 5.15: μ_{sat}, μ_{eff}, and μ_{FE} versus V_{GS} curves for a spin-coated ZnO TTFT fabricated using 25% zinc nitrate spin solution with a body thickness of 32 nm on a NEG/ITO/ATO substrate.

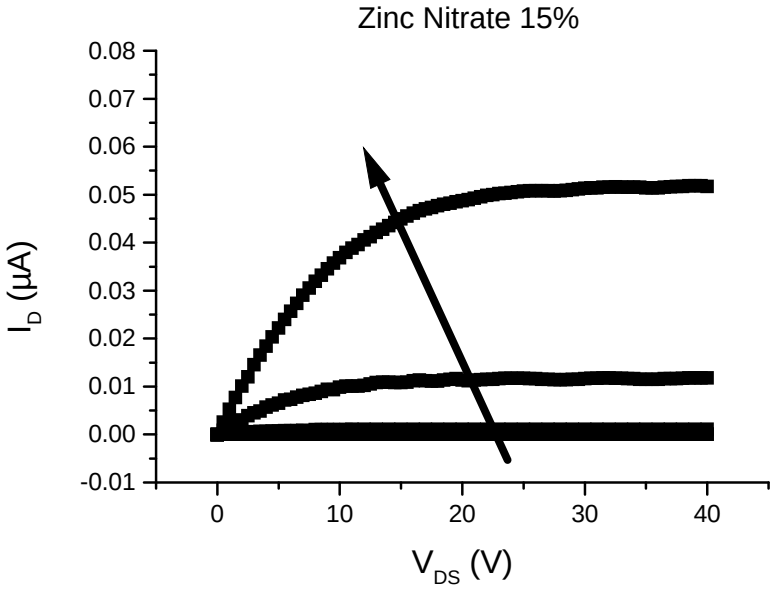

Figure 5.16: $I_D - V_{DS}$ curves for spin-coated ZnO TTFT fabricated using a 15% zinc nitrate spin solution with a body thickness of $\sim 15\ nm$ on a NEG/ITO/ATO substrate. Curves are shown for V_{GS} increasing from 0 to 40 V in 10 V increments as indicated by an arrow.

very small for all bias conditions. V_T, μ_{eff}, μ_{FE}, and μ_{sat} are calculated to be 21 V, $\sim$0.001, $\sim$0.001, and $\sim$0.001 cm^2/Vs, respectively. Additionally, $I_D - V_{DS}$ curves for a ZnO TTFT fabricated using 10% zinc nitrate solution, with a body thickness of $\sim 10\ nm$, indicate only gate insulator leakage current for all bias conditions tested. The body layers of spin-coated ZnO TTFTs made from 15% and 10% zinc nitrate solutions are so thin that the ZnO film is likely to be discontinuous, thus precluding electrical conduction through the body layer. Thus, the body conducts little or no charge even with a large gate bias.

The I_D on-to-off behavior for the TTFTs made from various spin solutions is shown in Fig. 5.17. The on-to-off ratios are 5.8, 133, 4.2×10^6, and 2.2×10^4 for TTFTs made from 100%, 50%, 25%, and 15% zinc nitrate solution, respectively. As expected, the I_D on-to-off performance improves greatly as the body thickness

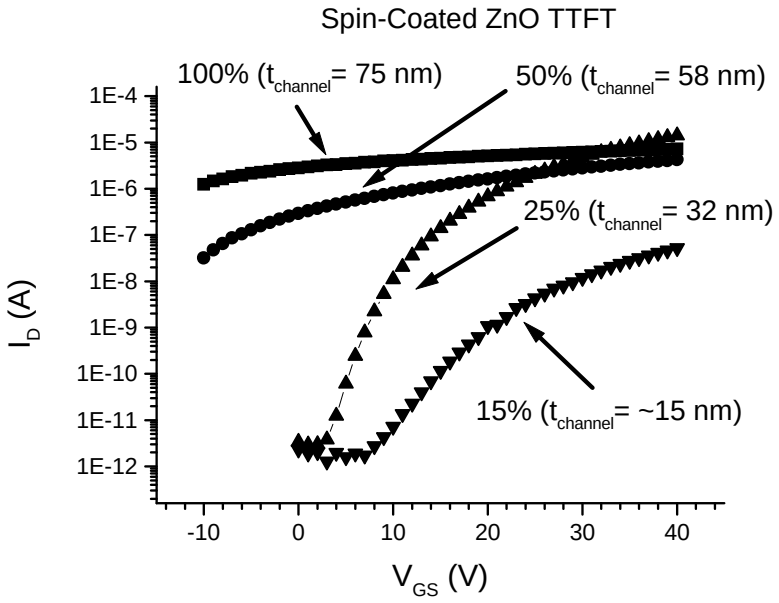

Figure 5.17: Semi-log $I_D - V_{GS}$ curves for spin-coated ZnO TTFTs fabricated on NEG/ITO/ATO substrates. Curves are shown for $V_{DS} = 40\ V$.

decreases, as it does for the TTFTs made using ion-beam sputtered ZnO. However, the I_D on-to-off ratio of spin-coated ZnO TTFTs also increases with thinner body thickness due to increasing mobility, at least for the 100%, 50%, 25% spin solutions. The TTFTs fabricated using the 15% and 10% zinc nitrate spin solutions do not follow this $I_D - V_{GS}$ on-to-off ratio trend since the ZnO body layers are apparently too thin to form continuous films.

ZnO spin-coated using a 25% zinc nitrate solution produced TTFTs with mobilities nearly as large as those obtained with ion-beam sputtered ZnO TTFTs. [120] Since a 25% zinc nitrate solution resulted in a thin-film with nearly the same thickness as the pore depth, as discussed in Sec. 4.2.1.4, it seems likely that the entire zinc nitrate layer converts uniformly to ZnO for this spin solution. Oxygen must diffuse through the zinc nitrate layer to convert the bottom portion of the zinc nitrate layer near the gate insulator, resulting in poor ZnO conversion of thick

zinc nitrate films near the gate insulator. Thus, it is likely that the low mobility of spin-coated ZnO TTFTs made from zinc nitrate solution thicker than 25% is a result of poor ZnO conversion near the gate insulator.

5.2.2 ZnO TTFTs From Zinc Acetate-Based Spin Solutions

Spin-coated ZnO TTFTs are prepared on NEG/ITO/ATO substrates and defined via photolithography using the zinc acetate-based spin solutions discussed in Sec. 4.2.3. ZnO bodies are prepared using 0.06 , 0.1, 0.2, 0.3 M zinc acetate-based spin solutions. The 0.2 and 0.3 M solutions resulted in ZnO thicknesses of 14 and 36 nm. The remaining solutions yielded ZnO thin-films too thin to be patterned via photolithography since ZnO films thinner than $\sim$ 10 nm cannot be seen with the alignment optics of the MJB3 mask aligner. Zinc acetate thin-films are baked at 115°C for 10 min on a hot plate and then converted to ZnO with a 600°C air oven bake for 10 min, as discussed in Sec. 4.2.3.

Neither the TTFT from the 0.3 M solution nor the TTFT from the 0.2 M solution produced transistor behavior, *i.e.* I_D is at gate insulator leakage current levels for all bias conditions. The XRD pattern in Fig. 4.13 shows that a ZnO thin-film from zinc acetate-based spin solution is not as well oriented as a similarly processed ZnO thin-film from zinc nitrate-based spin solutions. Thus, the TTFTs produced using zinc acetate-based spin solutions likely consist of poorly crystalized ZnO so that an effective channel cannot be induced by biasing the gate.

5.3 Spin-Coated HfO_2 Gate Insulator TTFTs

Bottom gate, source and drain on top TTFTs with HfO_2 gate insulators are constructed on Corning^{TM} 1737 glass substrates coated with ITO. The substrates are then coated with an $\sim$ 10 nm thick layer of SiO_2 via PECVD followed by a spin-coated thin-film of HfO_2, as discussed in Sec. 4.3. The remaining process steps are identical to those used for the ion-beam sputtered ZnO TTFTs, discussed in Sec. 5.1, but with a 134.5 nm thick ion-beam sputtered ZnO body. Spin-coated HfO_2 gate insulator TTFTs with 200 and 300 nm gate insulators are constructed along side of an ATO gate insulator TTFT so that the only difference between these TTFTs is the gate insulator construction.

The $I_D - V_{DS}$ and $I_D - V_{GS}$ curves of spin-coated HfO_2 gate insulator TTFTs, shown in Figs. 5.18 and 5.19, are similar to those obtained for ATO gate insulator TTFTs. μ_{eff}, μ_{sat}, and V_T are calculated to be 0.2 cm^2/Vs, 0.19 cm^2/Vs, and 22 V, respectively. The primary difference between spin-coated HfO_2 and ATO gate insulator TTFTs is that the mobility is slightly lower and V_T is higher for spin-coated HfO_2 gate insulator TTFTs. Additionally, changing the HfO_2 gate insulator thickness from 200 nm to 300 nm did not significantly effect the I_D on-to-off ratio indicating that spin-coated HfO_2 is pin-hole free at a thickness of 200 nm.

The difference in charge on the gate insulator of the HfO_2 and ATO gate insulator TTFTs responsible for V_T shift is calculated by

$$Q = C_i(V_T^{ATO} - V_T^{HfO_2}), \tag{5.2}$$

where C_i is the insulator capacitance per unit area of the gate insulator. By taking V_T of HfO_2 gate insulator TTFTs to be 20 V and V_T of ATO gate insulator TTFTs to be 10 V the charge on the HfO_2 gate insulator will be -2.89×10^{12} cm^{-2}. Notice that the same V_T shift could result from the same amount of positive charge on the

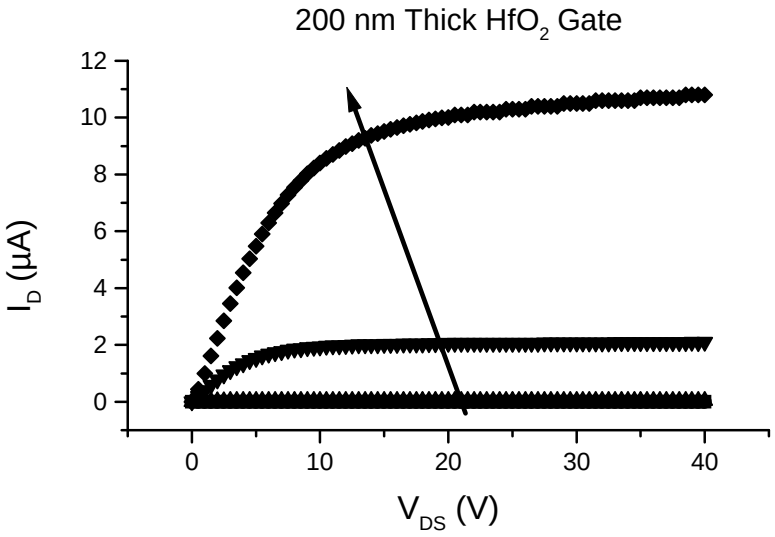

Figure 5.18: $I_D - V_{DS}$ curves for an ion-beam sputtered ZnO TTFT with a 134.5 nm thick body layer and a 200 nm thick spin-coated HfO_2 gate insulator. Curves are shown for V_{GS} increasing from 0 to 40 V in 10 V increments, as indicated by an arrow.

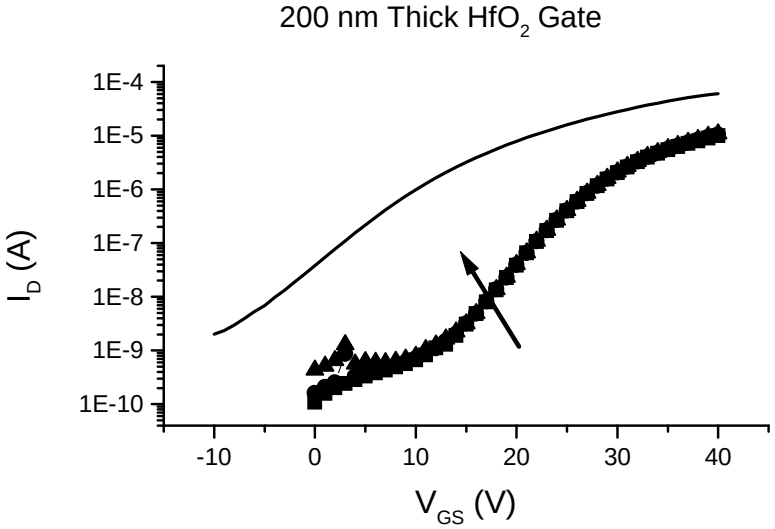

Figure 5.19: $I_D - V_{GS}$ curves for an ion-beam sputtered ZnO TTFT with a 200 nm spin-coated HfO_2 gate insulator and ion-beam sputtered ZnO TTFT with an ATO gate insulator (solid line). The ZnO body thickness is 134.5 nm for both devices. The ATO thickness is 220 nm. Curves are shown for V_{GS} increasing from 0 to 40 V in 10 V increments, as indicated by an arrow. V_{DS} is 30 V for the curve of the TTFT with the ATO gate insulator.

ATO gate insulator TTFT or a some positive and some negative charge on the ATO and HfO_2 gate insulator TTFTs, respectively. It seems likely that the spin-coated HfO_2 used in this study my have mobile ions since the starting material is a high purity. Also, since ATO and HfO_2 are very different materials it seems likely that interface states on the gate insulator ZnO interface would be very different. However, further study is necessary to assess if the source of this charge is from mobile ions, insulator trapped charge, insulator fixed charge, and/or interface trapped charge. [68]

5.4 SiO_2 Capped ZnO TTFTs

ZnO is know to chemisorb oxygen and create a depletion layer, as discussed in Sec. 2.7.1. Thus, having a ZnO TTFT in contact with an air ambient is presently essential to establishing a low carrier concentration in a ZnO body. However, it is desirable that ZnO TTFT performance is stable with regard to changes in ambient conditions. Additionally, interconnect layers must be constructed on top of TTFTs for integrated circuit applications. Thus, a method of encapsulating, *i.e.* passivating, the ZnO body region must be found. In order to assess the device physics issues related to encapsulated body devices, electrical properties of an SiO_2 capped ZnO TTFT are explored here.

A thin ($\sim$ 15 nm) layer of SiO_2, *i.e.* a cap, is deposited via PECVD onto bottom-gate, spin-coated ZnO TTFTs. Source and drain contact through the SiO_2 layer is accomplished by increasing the microprobe scrub length to scratch through the SiO_2 layer. The $I_D - V_{DS}$ curves shown in Fig. 5.20 are for a ZnO TTFT made from a 25% zinc nitrate solution; electrical characteristics for this device prior to depositing the SiO_2 cap are similar to those shown in Fig. 5.13. The body layer

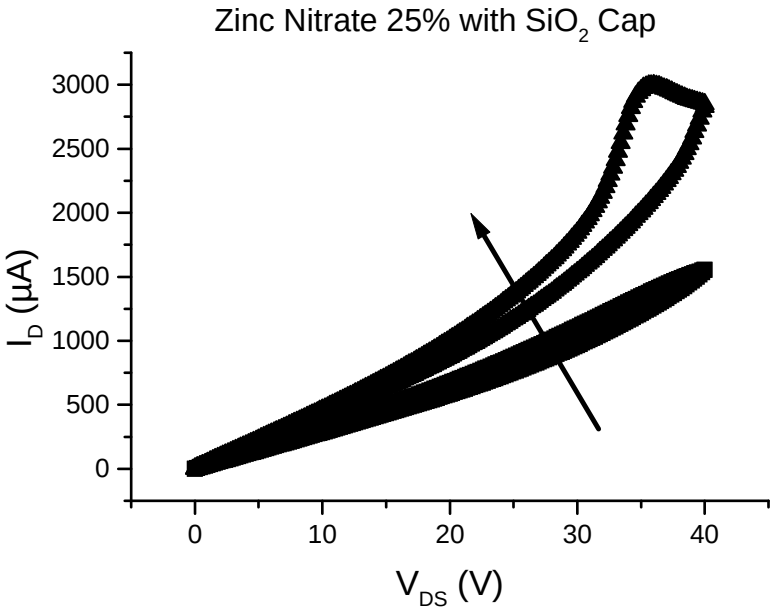

Figure 5.20: $I_D - V_{DS}$ curves for spin-coated ZnO TTFT fabricated using 25% zinc nitrate spin solution with a body thickness of 20 nm on a NEG/ITO/ATO substrate with a PECVD SiO_2 cap layer. Curves are shown for V_{GS} at 0 and 20 V. The arrow indicates V_{GS} increasing. Notice that both curves exhibit clockwise hysteresis.

becomes highly conductive with the deposition of the SiO_2 cap, layer so that I_D is large for any applied V_{GS}. Although there is some gate control of I_D, indicating gate charge modulation, the TTFT electrical characteristics provide no evidence of saturation. Also, counter clockwise hysteresis of the $I_D - V_{DS}$ curves indicates charge trapping within the body layer. The gate insulator current is at leakage levels for all applied biases; thus, the $I_D - V_{DS}$ hysteresis cannot be due to gate charging.

In light of the energy band diagrams discussed in Sec. 2.7.2 it is evident that the SiO_2 cap strongly accumulates the ZnO body. Prior to deposition of the SiO_2 cap, chemisorbed oxygen depletes the ZnO surface, as discussed in Sec. 2.7.1. Deposition of the SiO_2 cap apparently modifies the ZnO surface boundary condition, eliminating the chemisorbed oxygen and corresponding surface depletion, replacing it with a surface accumulation layer, as shown in Fig. 5.21. This suggests that

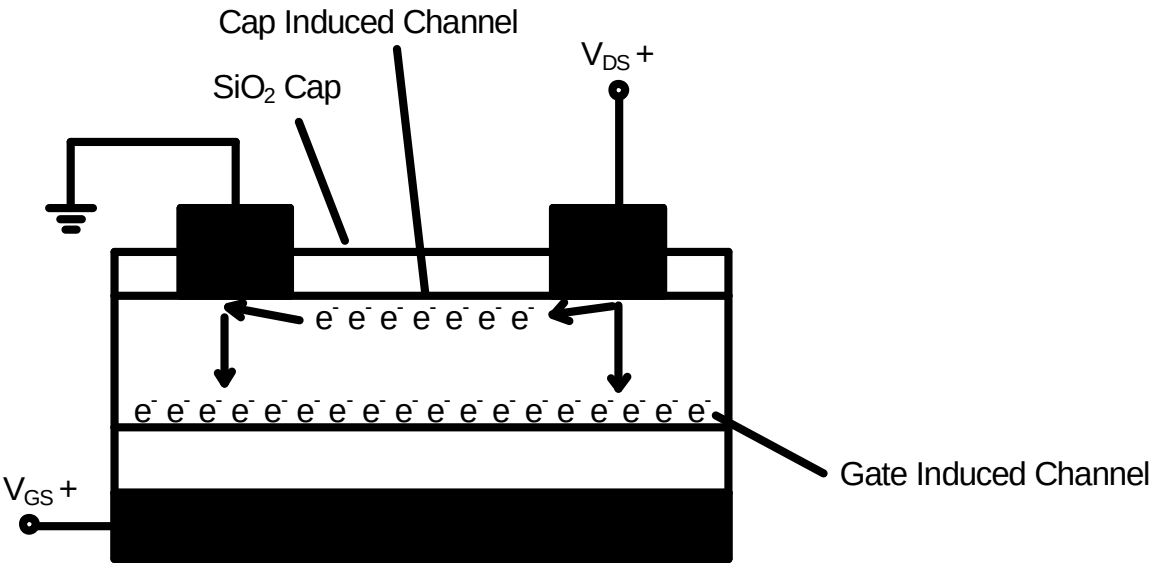

Figure 5.21: A schematic of an SiO_2 capped TTFT. The arrows indicate the direction of current follow and e^- indicates the presence of an electron channel.

surface depletion by chemisorbed oxygen is crucially important for enhancement-mode TTFT behavior.

Capping with spin-coated HfO_2 is also attempted. However, since the Hf spin solutions used in this dissertation are very acidic (PH $\leq$ 0.2) the spin solution completely etches the ZnO body during spin coating. Thus, the Hf spin solutions used in this dissertation cannot be directly spin-coated on top of ZnO.

5.5 Conclusions

Table 5.1 summarizes important general results of this chapter. Notice that some substrate-to-substrate variation exists between devices fabricated in a similar way, *i.e.* the 78 *nm* thick body ion-beam sputtered TTFT and the 220 *nm* ATO

gate insulator TTFT. Also, notice that the $I_D - V_{GS}$ on-to-off ratio increases as the body thickness decreases.

A photolithography process for ion-beam sputter ZnO TTFTs is demonstrated. Small device dimension TTFTs defined by photolithography perform in a similar way to larger TTFTs defined by shadow masking. However, as ZnO TTFT device dimensions and body thicknesses are decreased, I_D current limiting, likely as a result of source resistance, becomes increasingly problematic. Additionally as the body thickness increases, the $I_D - V_{GS}$ on-to-off ratio decreases, as a result of body bulk conduction.

Spin-coated ZnO TTFTs with electrical characteristics similar to those obtained for ion-beam sputtered ZnO TTFTs are demonstrated for the first time. Zinc nitrate spin solutions resulting in ZnO film thicknesses of 32 nm produce the best TTFT electrical characteristics of the spin-coated ZnO TTFTs fabricated to date.

Spin-coated ZnO TTFTs produced using zinc acetate-based spin solutions result in leakage level drain currents for all V_{GS}. XRD results show that the ZnO produced using zinc acetate-based spin solutions is poorly crystallized. Poor ZnO crystallinity results in poor TTFT channel mobility. Thus, the ZnO produced using zinc acetate-based spin solutions in this dissertation is likely so poorly crystalized that an effective channel cannot be formed for any applied V_{GS}.

The first spin-coated HfO_2 gate insulator ZnO TTFT is demonstrated. The electrical characteristics of HfO_2 gate insulator ZnO TTFTs are comparable to those of ATO gate insulator ZnO TTFTs. The primary difference between HfO_2 gate insulator and ATO gate insulator TTFTs is that the mobility is slightly lower and V_T is higher for HfO_2 gate insulator TTFTs.

SiO_2 capped TTFTs result a conductive ZnO surface accumulation channel so that the TTFTs can not be turned off, even with the application of a large negative bias to the gate. In this SiO_2-capped structures chemisorbed oxygen is not present at the ZnO surface, so that the ZnO surface is not depleted. Rather, a ZnO surface accumulation layer, as discussed in Sec. 2.7.2, is formed when a SiO_2 cap is deposited onto the ZnO surface, thus shunting the gate-induced channel and rendering the TTFT useless as a transistor.

Table 5.1: A summary of ZnO TTFT electrical characteristics.

TTFT process	Body Thickness (nm)	μ_{eff} (cm^2/Vs)	μ_{EF} (cm^2/Vs)	μ_{sat} (cm^2/Vs)	V_T (V)	I_D on-to-off ratio	Figs.
Ion-Beam	78	0.49	0.51	1.1	-3	316	5.1, 5.2, 5.3, 5.10
Ion-Beam	333	0.19	0.21	0.21	6–12	15	5.4, 5.5, 5.6, 5.10
Ion-Beam	20	0.82	0.95	0.95	1–3	8.6×10^5	5.7, 5.8, 5.9, 5.10
Zinc Nitrate 100 %	75	0.01	0.02	0.02	-20	5.8	5.11, 5.17
Zinc Nitrate 50 %	58	0.009	0.01	0.014	-4	133	5.12, 5.17
Zinc Nitrate 25 %	32	0.14	0.2	0.16	16	4.2×10^6	5.13, 5.14, 5.15, 5.17
Zinc Nitrate 15 %	~ 15	~ 0.001	~ 0.001	~ 0.001	21	2.2×10^4	5.16, 5.17
Zinc Nitrate 10 %	~ 10	-	-	-	-	-	-
200 nm HfO_2	134.5	0.13	0.2	0.19	22	2.5×10^4	5.18, 5.19
300 nm HfO_2	134.5	0.35	0.36	0.29	25	2.4×10^4	-
220 nm ATO	134.5	0.28	0.38	0.47	~ 10	3×10^4	5.19

6. CONCLUSIONS AND FUTURE WORK

6.1 Conclusions

- A novel spin-coated ZnO thin-film deposition method based on glycine, zinc nitrate, and deionized water is demonstrated. Previous spin-coated ZnO studies are based primarily on zinc-acetate spin solutions. This is the first study to show that zinc nitrate-based spin solutions produce high quality ZnO thin-films. The highest quality ZnO thin-films from zinc nitrate-based solutions are obtained using a $600°C$ pre-bake followed by a $600°C$ RTA in O_2. Also, the optimal thin-film thickness for converting zinc nitrate to ZnO is $\sim 30\ nm$.

- A novel process for spin-coating HfO_2 onto ITO coated glass substrates is demonstrated. HfO_2 spin-coated onto ITO-coated glass has a dielectric constant of 12.1–13.5, a loss tangent of 0.411%, and a breakdown field of ~ 2.1 MV/cm, and a leakage current of 17.37 nA/cm^2 at a field of 1 MV/cm. The dielectric constant is comparable to that of ATO and the loss tangent and breakdown field are adequate for TTFT applications.

- A crude SrS:Eu ACTFEL device in which the SrS:Eu phosphor layer is spin-coated is demonstrated. Additionally, spin-coated MgS shows promise as a method of developing MgS.

- A photolithography process for ion-beam sputtered ZnO TTFTs is demonstrated. However, as ZnO TTFT device dimensions and body thickness decrease, I_D current limiting, likely resulting of a large source resistance, becomes increasingly problematic.

- The first spin-coated ZnO TTFT is demonstrated to have performance similar to that of previously reported ion-beam sputtered ZnO TTFTs. Spin-coated ZnO body layers are deposited using a novel glycine, zinc nitrate, and deionized water spin solution. The best device performance is obtained with a spin-coated ZnO body thickness of 32 nm.

- The first spin-coated HfO_2 gate insulator ZnO TTFT is demonstrated. The electrical characteristics of HfO_2 gate insulator TTFTs are comparable to ATO gate insulator TTFTs. The primary difference is that the mobility is slightly lower and V_T is higher for HfO_2 gate insulator TTFTs compared to ATO gate insulator TTFTs.

6.2 Future Work

6.2.1 TTFT Work

6.2.1.1 Passivation Problem

Passivation is the biggest problem facing ZnO TTFT operation and its subsequent integration into useful circuits. For practical applications, TTFTs must be insensitive to the environment. Bottom-gate ZnO TTFTs require exposure to an oxygen ambient for proper operation. Capping a ZnO body layer with SiO_2 results in a conductive body.

One possible solution to this problem is to find an insulator that intrinsically depletes the ZnO body. Experiments comparing capped ZnO TTFTs to ZnO TTFTs stored and tested in an inert ambient should help to sort out the true nature of the passivation problem. In addition, different cap materials should be compared in

order to assess if there is an interaction between ZnO and SiO_2 which is unique to SiO_2.

Another possible solution is to employ a double gate TTFT so that both sides of the TTFT body are controlled by an electrical bias, making it possible to deplete the backside channel. However, the added processing complexity make this option less attractive than single gate TTFT passivation.

6.2.1.2 Interconnects

In order to construct TTFT integrated circuits it is essential that TTFTs can be connected together via interconnects. For the most part, this is a straightforward exercise in process integration, but problems do exist. Since methods for patterning ITO are established, see Sec. 3.2.6, the primary problem will be to create vias through the interlayer dielectrics. In Si integrated circuits, tungsten plugs are deposited in vias to insure contact through the interlayer dielectric. However, an equivalent method for creating a transparent plug does not exist and needs to be developed.

6.2.1.3 Transparent Passive Circuit Elements

Except for inductors, passive circuit elements in TTFT technology should be trivial to develop. MIM capacitors can be constructed using the gate contact as the bottom electrode, the gate insulator as the capacitor insulator, and the source/drain ITO as the top contact. A transparent resistor would be slightly more difficult to produce than a capacitor. Thin-films of ITO or lightly doped ZnO could be used the resistive element. However, it may be difficult to reproducibly control the resistance on a device-to-device and substrate-to-substrate basis.

The realization of transparent inductors was briefly explored during the course of the research pursued for this dissertation via patterning ITO-coated Corning^{TM} 1737 glass. However, the resulting spiral patterns have a small impedance and inductance. By placing the inductor on top of an iron plate (a high-permeability ferromagnetic material) the inductance device becomes significant compared to the impedance. Thus, a transparent ferrite material should be used in the construction of the inductor in order to increase the inductance to a useful value. A ferrite is desirable for this application since such materials possess both high magnetic permeability and a high resistivity, unlike most ferromagnetic which have a low resistivity. However, a transparent inductor requires a transparent ferrite; a suitable transparent ferrite is not currently available.

6.2.1.4 DRAM Demonstration

After successfully demonstrating interconnects and transparent capacitors, it would be useful to demonstrate a transparent DRAM cell. [121] Construction of a transparent DRAM cell would show that TTFT technology is implementable in a commonly used circuit configuration. In addition, a DRAM is a basic building block of an AMLCD pixel element. Thus, a transparent DRAM demonstration would aid in assessing how TTFT technology could be used to improve AMLCDs. The integration and processing methods necessary to implement a transparent DRAM are also necessary to construct a wide variety of transparent integrated circuits.

6.2.1.5 Active Pixel Demonstration (A Transparent Display)

The realization of an active-matrix transparent electroluminescent display appears feasible with the advent of TTFT technology. TTFTs could make up the

active-matrix drive portion of a transparent electroluminescent display. Organic light-emitting devices (OLEDs), as briefly discussed in Appendix A, offer many advantages as transparent display elements. Nontransparent organic smart pixels have been previously proposed and demonstrated. [122]

The organic layer used in OLED displays is thin ($\sim$ 100 nm) and has a band gap that is similar to that of visible light, so that the organic phosphor layer has a slightly colored transparent appearance. ITO is widely used as an anode contact in OLED technology; thus, OLEDs are compatible with the source, drain, and gate contacts currently used for TTFTs.

Three major hurdles exist, however, before transparent electroluminescent displays utilizing OLED pixels and TTFT switching transistors can be realized. First, OLEDs require current densities in the range of $\sim 200\ mA/cm^2$. Thus, a $1\ mm \times 1\ mm$ pixel would require $\sim 2\ mA$ of current. The best ion-beam sputtered ZnO TTFT with a width-to-length ratio of 8, driven at V_{GS} and at V_{DS} equal to 40 V, produce a drain current of $\sim$100 μA. Thus, for a similar ZnO TTFT to produce 2 mA a width-to-length ratio of at least 160 is required. Assuming the TTFT device has a 10 μm channel length (L), 1.6 mm channel width (W), and a source and drain width (L_S) of 50 μm the TTFT area [(L+2L_S)$\times$W] would be 0.176 mm^2. Notice that the TTFT area is much less than the 1 mm^2 area of the pixel. As TTFT mobilities improve, the width-to-length ratio required for this application would concomitantly decrease. However, these integration problems cannot be worked out using shadow masks since a device with a width-to-length ratio of 160 defined by shadow masking is larger than most glass substrates since the minimum shadow mask dimension is $\sim 0.5\ mm$.

The second major challenge for a transparent display is the passivation problem. Presumably, an OLED cannot be processed on top of a ZnO TTFT without

destroying the transistor properties. Also, since the organic layers used in OLED manufacturing typically cannot withstand more than $\sim 200°C$ without being destroyed, it is not possible to deposit TTFTs on top of an OLED pixel, thereby circumventing the passivation problem.

Finally, the low work function metals required for the cathode of OLEDs are invariably opaque. It is a nontrivial undertaking to make a transparent low work function conductor. A simpler solution may be to construct a very thin low work function cathode contact and to then cap it with a transparent conductor. Thus, the low work function cathode metal would be so thin that little light would be absorbed as it transits through the cathode metal. The oxygen sensitivity of low work function materials limits the way in which these materials may be processed, as considered in Appendix A. Thus, depositing a transparent oxide on top of an oxygen-sensitive material is not likely to work. Another possibility is to use a low work function material such as LaB_6 as a transparent contact, capping it with ITO. Both of these materials can be processed by RF sputtering, and could be deposited in a two gun RF sputtering system so that the cathode is not exposed to oxygen between depositions.

6.2.2 New Spin-Coating Materials

6.2.2.1 Multiple Spin-Coated Layers

Coating ZnO thin-films via multiple spin-coats of zinc nitrate warrants further exploration. It is unclear why multiple layers of zinc-nitrate based spin solutions do not build up thicker layers, as discussed in Sec. 4.2.2. It is possible that by spinning multiple layers of ZnO from spin solutions thicker than 15% zinc nitrate

spin solutions may build upon each other. Multiple layer spin-coats of HfO_2 produce thin-films with thicknesses of almost exact increments of a single spin deposition, as discussed in Sec. 4.3. Thus, it seems reasonable that the same method could work for spin-coating multiple layers of ZnO.

6.2.2.2 Insulators

The HfO_2 work presented in Sec. 4.3 barely scratches the surface of possibilities for spin-coating of insulating materials. A literature search of the materials listed in Table 2.1 yields very few publications related to spin-coated insulators. The results presented in this dissertation appear to constitute the first work to explore the electrical properties of spin-coated HfO_2.

Spin-coated HfO_2 should continue to be optimized. The first step would be to spin HfO_2 from pure source material and from a solution without glycine. It is likely that the dark color of spin-coated HfO_2 is a result of impurities, and possibly incomplete glycine burn out. Annealing of HfO_2 is not optimized; it is likely that an optimized annealing procedure will produce higher quality HfO_2.

6.2.2.3 Body Materials

Again the body materials possible using spin-coating synthesis are evident, since the work discussed herein constitutes the first application of spin-coating deposition to the fabrication TTFTs. Some preliminary spin-coating work with Zinc tin oxide (ZTO) looks promising, and Chang has had great success with this material via sputter deposition. [123] In addition, the spin-coating methods presented in this dissertation could easily be adapted to materials such as In_2O_3 and SnO_2.

Very little work has been performed to dope ZnO to change its electrical properties for TTFT applications. Doping is easily accomplished using spin-coating deposition, with a large variety of possible source materials. Typically the dopant source material is added to the spin solution in such a small quantity that the solution properties are not significantly altered and the solubility limit of the solvent is not reached. Thus, a large set of solutions with different doping concentrations could be attempted very quickly. The same experiment with sputtering would require the manufacture of a new target for each doping type and concentration, or the use of a source layer for diffusion doping. Source-layer diffusion-doping is more practical than doping of a sputter target, but the concentration is not as well controlled and some materials do not work as source layers.

6.2.2.4 Transparent Conductors

Transparent conductors have been widely explored by liquid-phase deposition methods but there is still room for more work. The spin-coated ZnO obtained using the zinc nitrate spin solution, as descrided in this dissertation, could be easily doped with Al, resulting in a transparent conductor. The current theory explaining the conductivity/thickness dependance of ZnO, as discussed in Sec. 2.6, does not explain the relatively high mobility of ZnO-based TTFTs. Resistivity (ρ) may be expressed as

$$\rho = \frac{1}{q\mu n}, \tag{6.1}$$

where q is the charge of an electron, μ is the mobility, and n is the carrier concentration. The prevailing conductivity/thickness dependance theory asserts that the high resistivity of a thin ZnO film results from the low mobility of a thinner film due to poor crystallinity. [26, 82] Thus, the ZnO mobility would have to change by

many orders of magnitude to explain the the resistivity versus ZnO thickness data. However, ZnO TTFT and bulk ZnO mobilities are within an order of magnitude of each other. A better explanation may be that thin layers of ZnO are completely depleted by chemisorbed oxygen at the the air ZnO interface whereas thicker films are only partially depleted so that the average carrier concentration in the film increases with film thickness. A few experiments exploring ZnO:Al thickness versus conductivity and ambient gas could help to clarify this. Spin-coating deposition is a good method to sort this out since repeated coats could be used to build up layers of variable thickness.

6.2.2.5 ACTFEL Devices

The spin-coating methods applied to ACTFEL devices just scratch the surface of possibilities of phosphor spin-coating development. The ACTFEL device discussed in Sec. 4.1 was not optimized. A series of experiments optimizing the sulfidization step and the dopant concentration should greatly improve the phosphor performance. In addition, increasing the phosphor thickness to $\sim 500\ nm$ and adding a top insulator would greatly improve the electroluminescent performance. Preliminary work to spin-coat MgS via MgO shows promise. Also, the spin-coating method for depositing ZnO discussed in this dissertation could be used to deposit ZnS by converting ZnO to ZnS using the same sulfidization process employed for SrS. [124]

The possibility of using in situ doping, *i.e.* dopant in the spin-solution, also is worth investigating. However, it is essential that the starting material and process

is clean and free of contamination before a meaningful spin-solution doping study may be performed.

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APPENDICES

A. ORGANIC LIGHT EMITTING DEVICES (OLEDS)

A.1 Introduction

Organic light-emitting devices (OLEDs) have recently become an exciting area of research and may soon become a widely used commercial electroluminescent (EL) display technology. [125, 126, 127, 128] The purpose of this appendix is to summarize the OLED capabilities at Oregon State University and to provide an introduction for integration of OLED technology with TTFT technology.

OLEDs in their most basic form consist of a organic phosphor deposited onto an ITO-coated glass substrate and capped with a low work function metal contact, as shown in Fig. A.1. ITO is a good hole injector into organic phosphors, and thus constitutes the anode. Low work function metals such as Ca or Mg are good electron injectors for organic phosphors, and thus form the cathode. Injected holes and electrons drift toward each other and recombine, which may result in photon creation. Light exits the device to the viewer through the ITO and glass substrate.

OLEDs may be divided into two general categories: small molecule and polymer based devices. Small molecule devices consist of phosphors of relatively small molecular weight and are typically deposited via thermal evaporation, whereas polymer based devices utilize a polymer as the light-emitting phosphor and are deposited via spin-coating. Polymer based OLEDs are often referred to as polymer light emitting devices (PLEDs). The Oregon State University laboratory facilities are best suited to PLED processing.

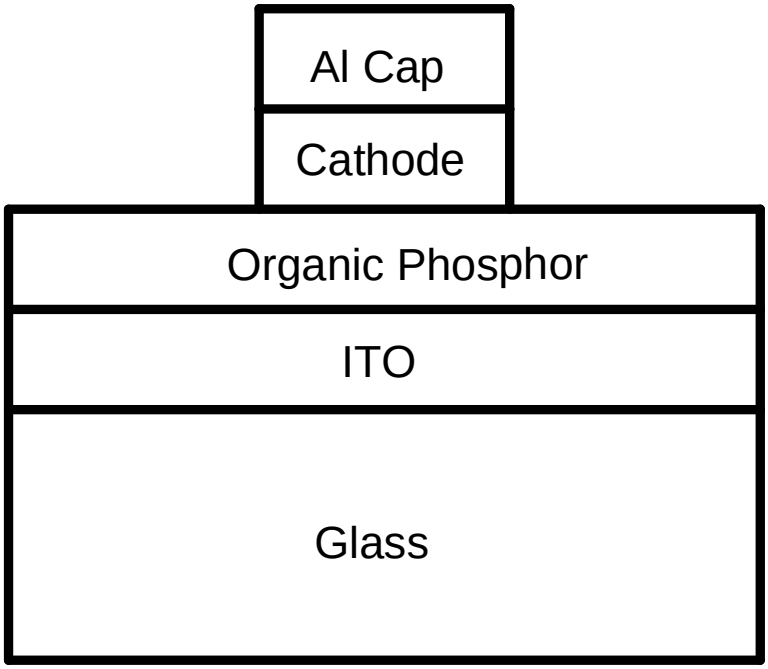

Figure A.1: A typical PLED structure.

A.2 Oregon State University PLED Processing Laboratory Description

The Oregon State University PLED processing facilities consists of a Brewer Science model 100 spin-coater and a modified M Braun glovebox, as shown in Fig. A.2. The glovebox is capable of maintaining water and oxygen levels less than 1 ppm and is equipped with a thermal evaporator and a vacuum oven capable of a maximum temperature of $600°C$. The thermal evaporator is pumped by a rotary vane vacuum pump and an oversized Cryo-pump. The thermal evaporator has excellent pumping speed and base pressure, $< 1 \times 10^{-6}$ torr in $< 15\ min$ from atmospheric pressure. It is uniquely capable for depositing high quality water and oxygen sensitive thin-films via thermal evaporation.

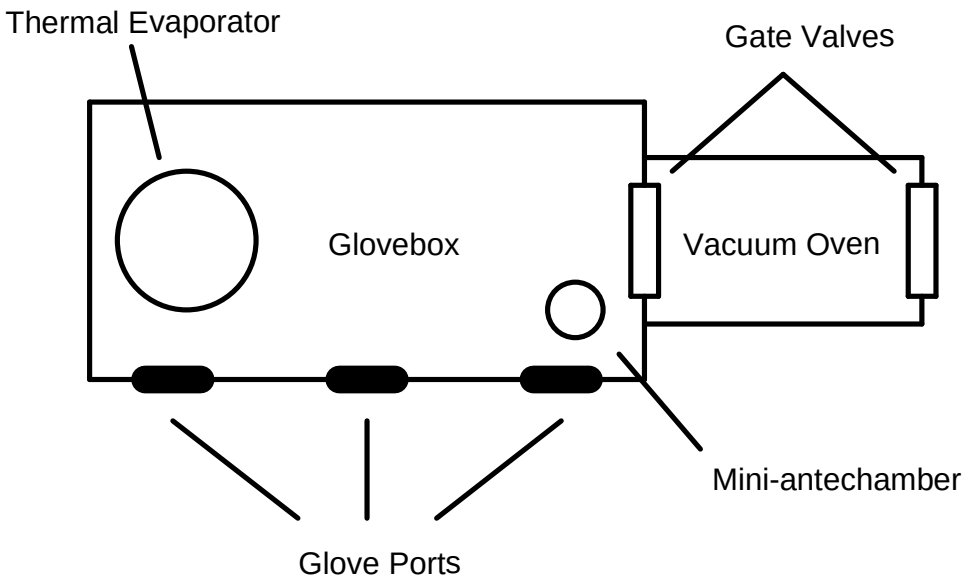

Figure A.2: A top-view of the modified M Braun glovebox available at Oregon State University.

A.3 Typical PLED Process

A.3.1 Spin Solution Preparation

The PPV precursor, *i.e.* p-Xylylenebis(tetrahydrothiophenium chloride), for PPV, *i.e.* poly(p-phenylenevinylene), may be purchased from Sigma-Aldrich. [129] A large variety of polymers for PLED use are now available commercially and PPV is not necessarily the best PLED polymer. The following procedure has been successfully used to synthesize PPV precursors for PLED use:

1. Add 2 g of PPV precursor to 12 mL of deionized water and stir.

2. Filter the solution to remove any undissolved particles.

3. Add 8 mL of 0.25 M NaOH solution and stir for 20 min. The viscosity of the solution will noticeably increase, resulting in a syrup-like consistency.

4. Add $\sim 2\ mL$ of 1 M HCl solution. The solution should have an approximately neutral PH at this point; if not, add acid or base as necessary.

5. Dialyze the solution against a 90% methanol 10% deionized water solution for 12 hrs and then repeat. The remaining solution should be clean, clear, and viscous.

A.3.2 Deposition and Anneal

Typically the PPV precursor solution is spun at 3000 rpm for 30 sec followed by a 500 rpm for 60 sec drying spin. Immediately following the spin, the substrate is placed in a vacuum oven and baked at $260°C$ for 2 hours. The substrate is then removed from the oven directly into the inert atmosphere of the glove box.

A.3.3 Cathode Deposition

Since OLED cathodes are typically fabricated using low work function metals, they must be deposited and handled in an inert atmosphere to prevent oxidation. Typically, the low work function cathode is capped with Al to offer some protection from oxygen and water. Metallic Ca makes a good cathode contact for PPV. Ca is thermally evaporated through a shadow mask to a thickness of $\sim 50\ nm$. Next a $\sim 70\ nm$ Al cap is thermally evaporated through the same shadow mask as the Ca contact. At this point the PLED device is complete and is capable of withstanding brief exposure to an air abient.

A.4 Electro-optic Characteristics

PLED electrical testing is accomplished by measuring the applied voltage, current, and light output; see Norris for a more detailed description of OLED charac-

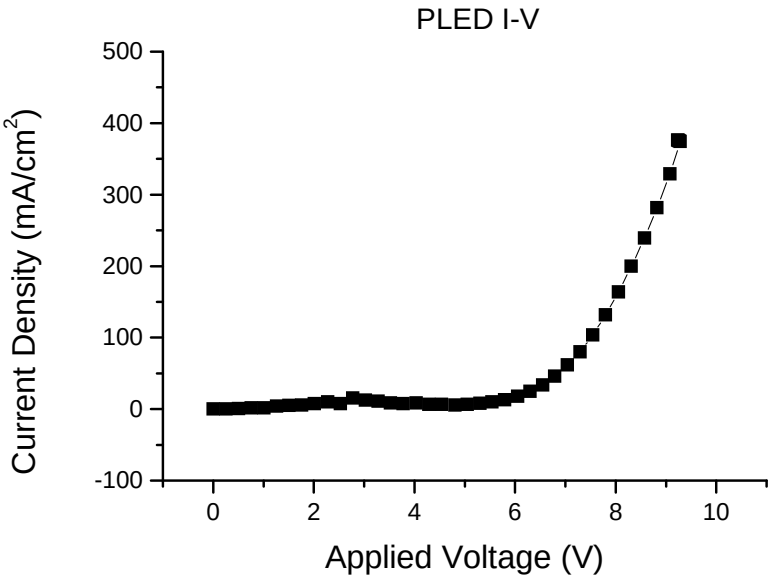

Figure A.3: A representative DC I-V curve of an Al cathode PLED constructed at Oregon State University.

terization methods. [127] Typically PLEDs are tested in a vacuum box to minimize cathode and polymer damage due to the air abient. Figure A.3 shows a typical PLED DC I-V curve. The light output is directly proportional the the current, and the device behaves as a diode, *i.e.* only conducting current when the bias is such that electrons and holes are easily injected from the cathode and anode, respectively.

B. PECVD INSULATOR PROCESSING

Processing a pinhole-free insulator via PECVD presents many challenges that often go unnoticed. Specifically the PECVD system in the Oregon State University cleanroom, as shown in Fig. B.1, possesses some peculiarities that every user should be aware of. When the procedures presented here are closely followed, PECVD is a reliable method for producing pinhole-free SiO_2.

PECVD of SiO_2 is an inherently dirty process. Over time a build up of SiO_2 powder occurs on the walls of the process chamber. This powder is easily dislodged from the chamber walls, and may land on the substrates to be coated. Thus, pinholes may be created in the SiO_2 film. In addition, the SiH_4 gas lines, mass flow controllers (MFCs), and other components can become plugged with a similar powder. Also, powder from the SiH_4 line may enter the chamber and land on the substrate via the showerhead and generate pinholes in the deposited SiO_2 film.

Most of the particle contamination problems may be eliminated by carefully wiping the inside of the chamber walls down with methanol before operating the PECVD (make sure that the bottom electrode is cold first). [130] However, when the build up has become so thick that a methanol wipe is not adequate, a freon etch should be used to completely remove all film build up. After a freon clean the chamber should again be wiped down with methanol. Finally, a $\sim 1.4\ \mu m$ thick layer of SiO_2 should be deposited before processing, *i.e.* the chamber should be seasoned. This seasoning layer is necessary to establish stable PECVD operation.

The PECVD system at Oregon State University, shown in Fig. B.1, has an adjustable top electrode. If the top electrode is not properly locked in place, via the locking ring on top of the vacuum chamber, the the top electrode will slowly sink over time (this could be over a period of years). Eventually the top and bottom

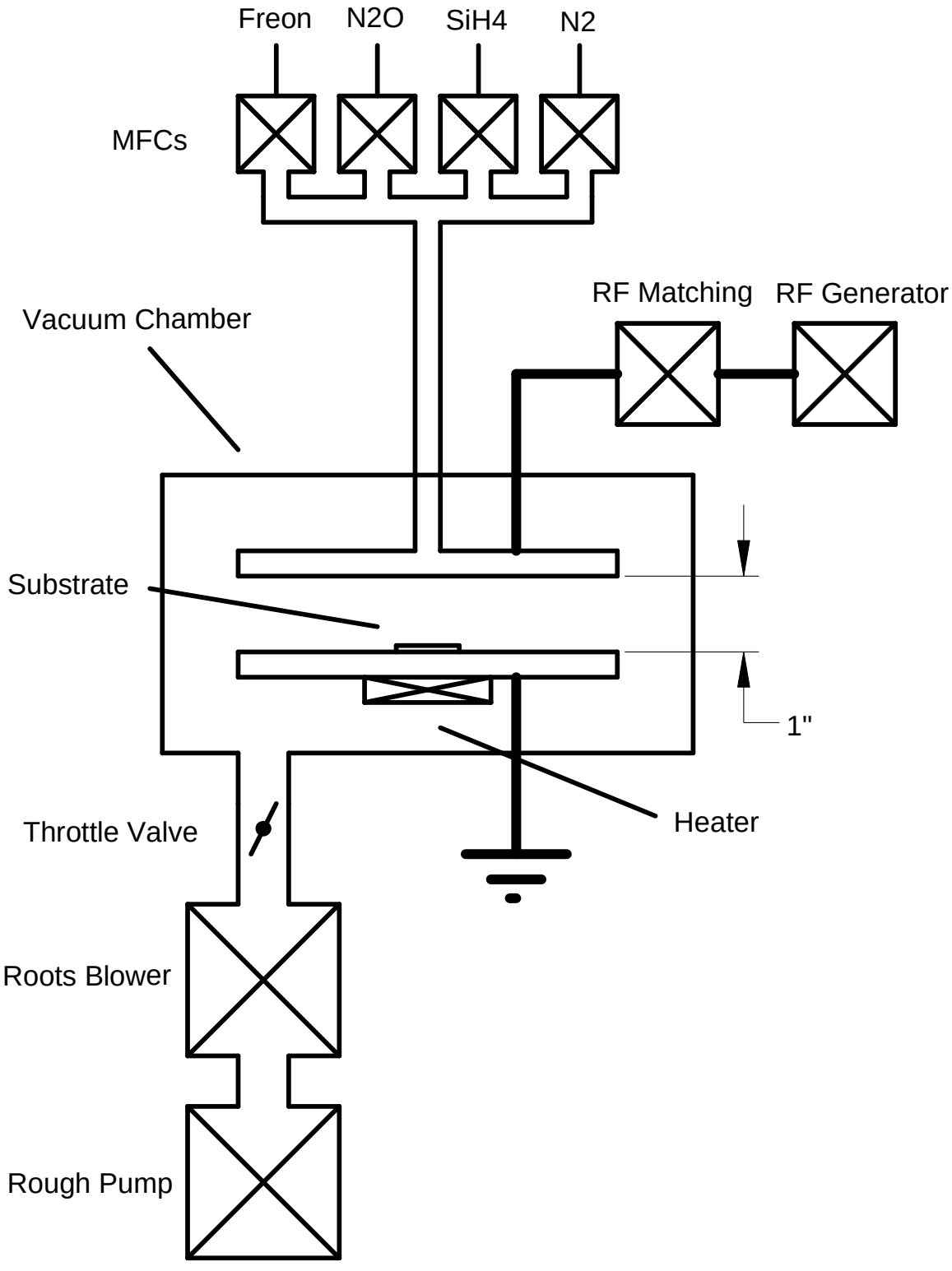

Figure B.1: A schematic of the PECVD system at Oregon State University.

electrodes are so close together that the plasma becomes unstable, and eventually the electrodes will short out. This could damage the RF power supply, cause matching problems, result in a flickering plasma, and/or cause the plasma to go out. If any of these symptoms occur, the electrode spacing should be checked. A spacing of 1" produces stable plasmas. The spacing is set by placing 1" spacers on the bottom electrode with the locking ring loose, then shutting the chamber and locking the top electrode locking ring.

When these procedures are followed the PECVD system at Oregon State University consistently produces SiO_2 films with breakdown fields $> 2MV/cm$. The SiO_2 recipe is relatively insensitive to gas flow, pressure, and electrode power. Thus, the SiO_2 recipe should be considered a good recipe to qualify the PECVD system since if this recipe does not produce good SiO_2 films there is likely to be a problem with the system.

B.1 SiO_2 Deposition Recipe

Process Gas: 2% SiH_4 98% He at 100 *sccm* and N_2O at 50 *sccm*

Pressure: 600 *mtorr*

Power: 125 W

Temperature: 350°C

Time: Dependent on desired film thickness.

Deposition Rate: ~ 10 nm/min

B.2 SiO_2 Seasoning Recipe

Process Gas: 2% SiH_4 98% He at 200 *sccm* and N_2O at 50 *sccm*

Pressure: 600 *mtorr*

Power: 125 W

Temperature: 350°C

Time: 70 min

Deposition Rate: $\sim$ 20 nm/min

B.3 Freon Etch Recipe

Process Gas: 92% CF_4 8% O_2 at 40 $sccm$

Pressure: 500 $mtorr$

Power: 200 W

Temperature: Unheated

Time: $\sim$ 2 hrs

Note: The freon etch should be repeated as necessary until the reaction chamber is clean.